Problems and solutions for clocks and clocking

Brian Bailey - September 25, 2012

The most prevalent form of design is synchronous design. This relies on a clock to latch in the results of the previous set of computations ready for the next step. This design paradigm helps to simplify the design process and has provided a level of abstraction that has been the mainstay of digital design for over 20 years. None of that is likely to change in the near future. When the methodology was initially put in place, wires were cheap in terms of area, performance impact and power consumed. That is not so today and the clock lines within a typical chip can consume a significant percentage of the total area and power. They have also become a significant source of headaches within the design process affecting manufacturing yield and causing significant headaches in terms of peak power and their impact on analog or other more sensitive circuitry. The significance of this became very to me recently when I was looking at the top most viewed design articles on the EDA Designline over the first year in which I was the editor. Many of the top ten articles were about clocks - the routing of them, the power impact of them, verification of clock domain crossings and many more.

So, I thought it would be a good idea to try and consolidate a number of articles about clocks together in one place. All of these articles appeared either in EDN or the EDA Designline within the past year, so all represent current papers.

**Fundamentals of Clocks and Clocking**, Analog Devices
The webcast covers the fundamentals of clock synthesis and distribution. It covers the various types of phase-locked loops (PLLs), the key features of these devices, and which end market they are designed for. Concepts such as reference switchover, holdover, phase noise, jitter, output drivers, and signal integrity are covered.

**Understanding clock domain crossing issues**, Saurabh Verma, Ashima S. Dabare, Atrenta
In today’s complex system on chip (SoC) designs, multiple clocks have become the norm. Thus, clock domain crossings (CDCs) are an integral part of any SoC. The main problems which can occur in a clock domain crossing are metastability, data loss and data incoherency. In this paper, all these issues for different types of synchronous and asynchronous clock domain crossings are discussed.

**Pitfalls to avoid in SoC clocking**, Vijay Bhargava and Harkaran Singh, Freescale Semiconductors
A careful observation of the clock structures and their implementation through the various stages of VLSI flow is of utmost importance. This paper illustrates few pitfalls which a VLSI designer should be aware of to achieve the optimal clock structure for the design.

**Configurable dividers for SOC- and block-level clocking**, Prateek Gupta and Priyanka Garg, Freescale Semiconductor
There is a need of clock divider circuitry that can generate divided clocks from the master PLL/oscillator clock or any system clock and feed different divided clocks to different device modules. As clocking can also be application driven, the clock dividers must be configurable. This article illustrates the various implementations of configurable clock divider logic used in SoCs today and highlights their challenges, advantages or limitations over the others.

**Designing a robust clock tree structure**, Amol Agarwal and Priyanka Garg - Freescale Semiconductor

Clock tree synthesis (CTS) is at the heart of ASIC design and clock tree network robustness is one of the most important quality metrics of SoC design. With technology advancement happened over the past one and half decade, clock tree robustness has become an even more critical factor affecting SoC performance. Conventionally, engineers focus on designing a symmetrical clock tree with minimum latency and skew. However, with the current complex design needs, this is not enough.

Please let everyone else know about other articles, papers or educational materials related to clocks. They don’t have to have been published here as I am sure it will be helpful to everyone to have a complete list of resources.

**Brian Bailey** – keeping you covered

If you liked this feature, and would like to see a weekly or bi-weekly collection of related features delivered directly to your inbox, sign up for the [IC Design newsletter](#).