Designers using high-speed data converters in systems that have FPGAs as receivers have traditionally struggled with the complexity of interfacing these complementary solutions.

In April 2006, JEDEC, the global leader in developing open standards and publications for the microelectronics industry introduced the JESD204 standard. This new standard defined a multi-gigabit serial data link between converters and a receiver (commonly FPGA or ASIC).
The original standard defined 1 lane, 1 link which defined transmission of samples across a single serial lane for multiple converters at speeds up to 3.125 Gbps. See Figure 1.

Designers greatly benefited from this in many ways:

- Overall system design was simplified leading to smaller/lower number of trace routes and easier to route board designs.
- Reduction in pin count on both the TX and RX side by Move from high pin count low speed parallel interfaces to low pin count high speed serial interfaces. In addition an embedded clock was incorporated to even further reduce pin count.
- Reduction in system costs came from smaller IC packages and simpler board designs.
- The standard was easily scalable to meet future bandwidth requirements. As geometries shrink and speed increases, the standard adapts.

In April 2008, JEDEC launched the first revision expanding of this standard to multiple links and multiple lanes as the standard moved to JESD204A. See Figure 2.
August 2011 brought further improvements to the standard with JESD204B, a second revision that utilized a device clock and added measures to ensure deterministic latency. See Figure 3.

Figure 2: The JESD204A revision adds capability for multiple aligned serial lanes for multiple converters at speeds up to 3.125 Gbps.

Figure 3: The JESD204B standard now supports multiple aligned serial lanes for multiple converters at speeds up to 12.5 Gbps.

JESD204 Simplified System View (See Figure 4)
JESD204B defines three normative Device Subclasses with respect to Deterministic Latency/Harmonic Clocking (DLHC):

- **No Support for Deterministic Latency (Device Subclass 0)**
- **Deterministic Latency Using SYSREF (Device Subclass 1)**
- **Deterministic Latency Using SYNC~ Detection (Device Subclass 2)**

Let’s take a closer look at Analog Devices choice for a high performance, high speed ADC that supports JESD204B-SC1.

AD9250: 14-Bit 250-Msps 1.8V Dual ADC with JESD204B outputs. Figure 5 shows a block diagram.
Figure 5: The block diagram of the AD9250 shows the added device clock lines

Analog Devices has created a high speed ADC FIFO evaluation kit that includes the ADC Analyzer and a buffer memory board to capture blocks of digital data from the AD9250 high speed analog-to-digital converter (ADC) evaluation boards. The FIFO board is connected to the PC through a USB port and is used with ADC Analyzer to quickly evaluate the performance of high speed ADCs. Users can view an FFT for a specific analog input and encode rate to analyze SNR, SINAD, SFDR, and harmonic information. See Figure 6.

These boards are able to handle multi-GHz frequencies with expert layout and grounding techniques and support components such as differential clocks that optimize the performance capabilities of high-speed ADCs.
Another useful development board is the Interposer card for the dual high speed ADC family. The AD-ADC-FMC-ADP adapter board allows any of Analog Devices' High-Speed ADC Evaluation Boards to be used on certain Xilinx® evaluation boards with a FMC connector. The adapter board uses the Low Pin Count (LPC) version of the FMC connector, so it can be used on either LPC or HPC hosts (such as the KC705 or VC707) See Figure 7.
JESD204B for ultrasound

The second key area in system design where the JESD204B standard is most effective is in the ultrasound receiver. ADI’s AD9671 octal ultrasound receiver IC takes advantage of the standard to eliminate the complex circuit board traces on the ADC bus in such a system of multiple ADCs.

Figure 8 shows an example of the complexity of a typical ultrasound system and the tremendous reduction of high speed circuit board pairs and simplification of circuitry.

In summary, JESD204B in ultrasound has these benefits:

- Simplify board routing, FPGA or ASICs
- Beam-forming in software, GPU, DSPs
- FPGA vendors offering GTX transceivers on multiple price point families like Xilinx, Altera and Lattice