Understand linear regulator stability

Sudhansu Sekhar Mishra, Tarun Rehani, and Nishant Thakur - November 26, 2012

A regulator is a closed-loop feedback system. For the LDO to be stable, the phase margin must be positive. In other words, at unity gain crossover frequency of the gain curve, the phase of the system should be positive. This can be measured using a vector network analyzer. Many voltage regulators are of the fixed output variety and include the voltage divider internal to the regulator. There are definite advantages to this approach, which allows active voltage trimming and also minimizes the physical space required. A disadvantage to this approach is that the voltage divider is not available for gain-phase or “Bode” measurement. This leads many to believe that it is not possible (or even necessary) to evaluate the stability of such a regulator. This is simply not true.

An empirical observation can be made to understand the relative stability of the feedback system and leverage that understanding to monitor low voltage detects and the transient performance of the system. It is important to keep the voltage regulator stable in order to make sure that the output voltage of the regulator does not go above and below specified limits and does not break into oscillations. SPICE simulation can be used to easily predict stability of the voltage regulator in both the time and frequency domains, but it is rather difficult to predict post-silicon on a validation board where only transient simulations can be done. Is it not possible to know exactly how much phase margin a voltage regulator loop has by merely looking at transient responses. However, the transient response can still be used to test whether the regulator is stable or not by observing ringing behavior at its output for a transient load current. It is necessary to pay attention and plan for necessary pins and circuit elements on board in order to apply different transient load currents at the regulator output to test its stability.

Types of regulators
Regulators can be built on the premise of a linear or non-linear regulator, depending on the underlying principles on which they work. The basic types are linear regulators (low drop-out regulators; LDOs) and non-linear regulators (also known as switching regulators, or switch-mode power supplies; SMPS). LDOs are used extensively because of their design simplicity, low footprint on a silicon wafer, and low noise whereas SMPS cater to higher current needs and higher efficiency.
The principle of an LDO is simple. A part of the output is fed back to the error amplifier through a resistor divider network, which makes the regulator function in a closed loop. That fraction of the output is compared with the reference voltage from the band gap reference generator. By controlling the current through the pass transistor, the output voltage is controlled. Hence, a steady voltage is attained at VOUT. The bypass capacitor ensures that if any fast transients are seen on the load, it is able to supply the same until the feedback loop compensates. This ensures there are no ripples in the load transients.

**Stability in the frequency domain**

A regulator is a closed-loop feedback system. So, for the LDO to be stable, the phase margin must be positive. In other words, at unity gain crossover frequency of the gain curve, the phase of the system
should be positive, non regenerative i.e. neither 0 nor multiple of 360. The LDO could be modeled as a control system with the error amplifier, pass transistor, and feedback resistor forming a closed-loop system. The output impedance model of the LDO depends on the bypass capacitor, bulk/stability capacitor, the equivalent series resistance (ESR) of the bulk capacitor, output impedance of the error amplifier, and parasitic capacitance of the trace to the base of the pass transistor. This model forms three poles and one zero. The location of poles and zeros can be calculated as shown below. (The Laplace transform could be used for calculations, and the following impedances will be in parallel.)

\[
R_{\text{out}} || \left( R_{\text{ ESC}} + \frac{1}{(sC_{\text{bulk}})} \right) || \left( \frac{1}{sC_{\text{bypass}}} \right)
\]

Where, 
- \(R_{\text{out}}\): Output Resistance of the Pass Transistor 
- \(R_{\text{ ESC}}\): ESR of the bulk capacitor 
- \(C_{\text{bulk}}\): Bulk/Stability capacitance 
- \(C_{\text{bypass}}\): Bypass capacitance

Simplifying the above equation, the poles and zeros could be found as shown below:

\[\frac{1}{2\pi(R_{\text{out}} + R_{\text{ ESC}}) \times C_{\text{bulk}}}\]

- \(P_1\): it is because of the presence of the output bulk capacitor and the output resistance of the pass transistor.
- \(P_2\): it is because of the impedance of Bulk capacitor and Bypass capacitor
  \[\frac{1}{2\pi R_{\text{ ESC}} \times C_{\text{bypass}}}\]
- \(P_3\): it is because of the ESR of Bulk capacitor and Bypass capacitor
- \(Z_1\): it is because of the ESR of Bulk capacitor and Bulk capacitor itself
  \[\frac{1}{2\pi R_{\text{ ESC}} \times C_{\text{bulk}}}\]

\(R_{\text{ PAR}}\) & \(C_{\text{ PAR}}\) are the parasitic impedances of the error amplifier's output stage and trace between the error amplifiers and pass transistors.

A typical pole zero location plot is shown in Figure 3. P1 is dominant pole and it depends on load current values (\(R_{\text{out}} = \frac{1}{(K \times \text{Drain current})}\) where \(K\) is channel length modulation parameter. As load current increases, \(R_{\text{out}}\) reduces and the pole moves to higher frequencies. The relative location of \(P_1\), \(P_2\), and \(Z_2\) determines the phase margin of the system. \(P_3\) is usually at very high frequency outside the unity-gain bandwidth of the system. A high value of RESR helps to bring \(Z_1\) near \(P_2\) and hence improves phase margin while also degrading the transient response (as explained in next section).

![Figure 3 Gain Plot of arbitrary LDO depicting the position of poles and zeros](image-url)
Stability concept in time domain (continued on www.tmworld.com)