Electronics design trends that ratchet up design complexity and speed, such as the use of multiple high-speed buses, bring new signal-integrity challenges. With that in mind, EDN assembled a virtual panel of engineers working in signal integrity to examine the current impairments, assess how well the available test equipment is measuring up, and determine what we can do both short- and long-term to improve signal integrity. Admittedly, there are many things that can affect signal integrity (Reference 1); in this discussion, we focus primarily on crosstalk and EMI.

What’s the problem?

Many a trained eye is focused on the effects of multiple high-speed buses on signal integrity and how to avoid the related problems. Chris Loberg, senior technical marketing manager at Tektronix Inc, and Tim Caffee, vice president for design validation and test at Asset InterTech Inc, agree that shrinking operating margins on high-speed buses are contributing to the challenges.

“The design trend is faster serial speeds, above 10 Gbits/sec, with no new cost-effective architecture for improving signal-path accommodation of issues like EMI and crosstalk,” Loberg observes. “So, signaling accommodations like equalization must be made to minimize EMI and crosstalk effects, enabling the receiver to accurately determine the serial-bus logic transition.”

Loberg notes that interval times—the time between a transition to one or zero—are shrinking; as a result, in a traditional eye diagram Image: Shutterstock used to evaluate transitions, EMI and crosstalk are “closing” the eye. Engineers can no longer effectively evaluate signal integrity, as crossing points and timing-integrity evaluations become much more challenging.

Caffee notes that with each successive generation of high-speed bus, operating margins are gradually shrinking as signal frequencies increase, enabling effects such as jitter, intersymbol interference (ISI), and crosstalk to “create havoc” on the signal integrity of high-speed SerDes and memory channels. Each new step to a higher speed and signaling frequency makes the bus more susceptible to distortions and anomalies that can effectively disrupt traffic and stall system throughput.

The eye diagram in Figure 1 illustrates this point, showing the effects of increasing signal frequencies on three generations of a hypothetical high-speed bus and the resultant, decreasing operating margins on the bus. As frequencies increase, even the slightest distortion can disrupt signaling throughput.
Alan Blankman, product manager for signal-integrity products at Teledyne LeCroy, agrees that higher bit rates (>25 Gbits/sec) and “parallelized serial” standards such as PCI Express (PCIe), 40/100GBase-R, and InfiniBand are contributing to signal-integrity issues. “Faster bit rates require faster edges with higher-frequency content, which results in bigger reflections due to impedance mismatches at connectors, vias, packages, etc.; higher levels of loss; and higher levels of crosstalk and EMI, due to increased coupling to neighboring traces,” Blankman says.
user is provided a one-button interface—is a sophisticated affair, taking into account clock recovery and knowledge of phase-locked loops, jitter decomposition techniques and assumptions for them, crosstalk and its effects, and waveform statistics that require different approaches" (Reference 2). Howard adds that the Agilent U4154A 4-Gbit/sec AXIe logic-analyzer module can make reliable measurements on eye openings as small as 100 psec × 100 mV (Figure 2).

Howard Johnson of Signal Consulting Inc concurs that circuits at very high speeds are notoriously difficult to probe. “Even in cases when a probe exists that can do the job, you often cannot place the probe at the point in a circuit that you wish to observe,” says Johnson. He suggests that the answer is to use cosimulation, or the process of simultaneously developing both a physical circuit and a software simulation of it.

The problem, observes Ransom Stephens of Ransom’s Notes, is that, despite new oscilloscope techniques from leading manufacturers, there is no automated way to identify crosstalk unambiguously. The latest test products offer ways to estimate the effect of crosstalk on the bit error rate (BER), but they are all process-of-elimination approaches.

“Avoiding crosstalk is simple in principle but sometimes impossible in practice,” Stephens acknowledges. Because crosstalk is caused by jolts of radiation when an aggressor signal makes a logic transition, increasing the rise/fall times will reduce crosstalk. Because it’s interference, increasing trace separation has a big effect, too.

“I think that careful differential design is your best bet, though,” Stephens offers. “If you can get the differential skew really small and get the two traces nearly on top of each other, then the cancellation from differential signaling has a fighting chance.”

How do we improve SI?

According to Tektronix’s Loberg, there are several ways forward. First, change and improve the signal path itself. One way to do that is with an optical backplane; this is happening, but not in the mainstream (think Thunderbolt). Another way to improve signal integrity is to trick the signal using equalization approaches to minimize crosstalk; for instance, you could hard-code the chip or compile FPGA code to equalize the signal. In addition, many designers are managing crosstalk and EMI through better design practices around the signal path.

Asset InterTech’s Caffee proposes that engineers validate signal integrity on the bus during each of the major phases of a system’s life cycle, from design to field operation, though he recognizes that this is a challenging approach and thus not a popular one. If detected during prototype-board bring-up, signal-integrity problems could trigger changes in the design; if detected during manufacturing, problems could result in alterations to the production process. If problems are detected in the field as a result of troubleshooting poorly performing systems, design changes, manufacturing-process changes, or both should be made for the next product generation to reduce returns and warranty claims.

Hiroshi Goto, business development manager at Anritsu Co, suggests pre-emphasis as an effective transmission technique for maintaining the eye opening. With transmission speeds increasing to 20 Gbits/sec and faster, Goto proposes a three- or four-tap emphasis signal in order to increase the number of bits to be emphasized.
It’s a complex job to check and set the combination of emphasis rates for each tap, however, making it difficult to find the ideal emphasis signal without quantitative guidelines.

The Anritsu-developed MP1825B four-tap emphasis and transmission-analysis software, working with the MP1800A signal-quality analyzer BER test set (BERTS), finds “the ideal emphasis settings based upon the reverse characteristics” of the device under test (DUT), says Goto (Figure 3). “This raises the height of the eye and keeps the eye open, allowing better quantitative signal-integrity analysis in the shortest amount of time.”

![Figure 3](image)

**Figure 3** The Anritsu MP1800A 32G synchronized multi-BERTS and MP1825B 28.1G four-tap emphasis aim to assist signal-integrity analysis by keeping the eye open.

**Simulation and validation**

Most agree that simulation is becoming mandatory for high-speed system design. Agilent’s Howard says the company’s Advanced Design System (ADS) is the leading EDA software in use for high-speed digital applications.

Teledyne LeCroy’s Blankman adds that to detect and mitigate crosstalk issues, designers must be able to predict near- and far-end crosstalk by running simulations, and to validate the models used in the simulations by taking measurements (Figure 4). To validate crosstalk models, designers need multidifferential-lane S-parameter measurements (eight-port for aggressor-victim models, 12-port for aggressor-victim-aggressor models, or even higher port counts).
Figure 4 The SPARQ signal-integrity network analyzers from Teledyne LeCroy connect directly to the DUT and PC-based software through a single USB connection for quick, multiport S-parameter measurements.

Measuring crosstalk requires vertical noise measurements taken by real-time oscilloscopes that can extract the crosstalk from the serial data signal. Those measurements should estimate eye closure as a function of BER, as jitter measurements do. Jitter measurements are also important, of course. Measuring both jitter and noise yields a more complete picture of crosstalk than jitter measurements alone.

Toolbox

Test-equipment vendors are working to evolve their tools to characterize jitter and improve signal-integrity analysis, so the optimal toolbox for signal-integrity engineers may not yet be available. Signal Consulting’s Johnson predicts that “the next trend will involve a blend of specialized equipment and test software designed to characterize a power system and inject specific test current waveforms into that power system.” Stephens, of Ransom’s Notes, suggests that we be on the lookout for more crosstalk-equalization techniques.

So, what’s out there now?

- Scopes. Here is where high-bandwidth oscilloscopes can really prove their worth. Teledyne LeCroy’s Blankman notes that nonreturn-to-zero (NRZ) serial data patterns can have rise times less than 30 psec. He points out that receiver testing of PCIe Gen3 systems requires a scope with a 13-GHz bandwidth, whereas transmitter testing needs a 20-GHz scope.

“Emerging multilane designs like InfiniBand and 40/100GBase-R have even more-demanding requirements for channel count and bandwidth,” Blankman says. “These standards utilize bit rates of 25 and 28 Gbits/sec. Typically, an oscilloscope with four or five times the fundamental frequency is needed, which corresponds to 50 to 65 GHz. Since InfiniBand and 40/100GBase-R are multilane, acquiring eight, 12, or even more channels at a time is required to fully characterize SI issues.” Blankman points to Teledyne LeCroy’s LabMaster 10 Zi, with bandwidth out to 65 GHz and a ChannelSync architecture that synchronizes up to 80 channels to operate as a single instrument.

Network analyzers
Network analyzers. Network analyzers are important for characterizing crosstalk in multilane systems and revealing the frequency characteristics of the DUT. Anritsu’s Goto points out that in order to acquire the best S-parameter data, the vector network analyzer should have broad frequency coverage. He suggests Anritsu’s VectorStar VNA, which ranges from 70 kHz to 125 GHz.

“While the upper frequency receives most of the attention,” he warns, “it is important to remember that accurate measurements to the lowest possible frequency are critical for signal-integrity applications. Often, the accuracy of models can be improved by measuring down to as close to dc as possible, providing the precise data to help create a high-accuracy eye diagram.”

Blankman notes that network analyzers with high port counts can be expensive. He says the network analyzers in Teledyne LeCroy’s SPARQ series (Figure 4) were designed for signal-integrity measurements and offer a lower-cost option to a traditional VNA. (SPARQ stands for “S-parameters quick.”)

Software. Given the need for more simulation, vendors are developing software tools to work with their hardware. Loberg notes the availability of serial-data-link analysis (SDLA) on the Tektronix scope (Figure 5), which can help engineers simulate equalization in EDA environments such as those from Cadence Design Systems or Mentor Graphics. “That software model can be dropped into an oscilloscope, transferring the model properties into the S-parameters; then we can place the effects of that effort into a filter on the scope,” Loberg explains. “The scope can then model the behavior of the equalizer into the signal being measured and see if we can open the eye. This approach allows you to analyze the performance with the effects of equalization baked into the scope.”

Figure 5 This screen image of serial-data-link analysis shows different eye diagrams before and after inclusion of equalization effects and channel/fixturing effects (courtesy Tektronix).
Teledyne LeCroy also offers oscilloscope-based serial-data-analysis software in its SDAIII-CompleteLinQ product. Blankman notes that it is important to have scope-based software that performs eye, jitter, and vertical noise analysis. He says users also need tool kits that allow fixtures and interconnects to be de-embedded or emulated, and that apply transmitter and receiver equalization. “The analysis tool kit should also provide a wide variety of plots that show the variation and distribution of jitter and noise in frequency and time in order to understand the root causes of noise and jitter,” Blankman adds.

• **BERT.** “Receiver testing is becoming mandatory in many standards, and most people don’t know where to start,” says Howard, who adds that system calibration—critical for ensuring the accuracy of your measurements—may be the hardest part of testing.

Howard reveals that in working with engineers, she has found proper calibration of the stress signal in PCIe 3.0 to be challenging. She points to the Agilent N4903B J-BERT high-performance serial BERT to test Rx compliance. The instrument can characterize a receiver’s jitter tolerance and is designed to prove compliance with today’s most popular serial-bus standards, including PCIe, SATA/SAS, DisplayPort, and USB.

Goto suggests that when selecting a BERT, engineers should choose one with minimal intrinsic jitter. For example, the Anritsu MP1800A has intrinsic clock jitter of <350 fsec RMS. The BERT should also be able to conduct repeatable and stable jitter-tolerance tests with a variety of generated jitter types, such as sinusoidal, random, and bounded uncorrelated jitter and spread-spectrum clock that can be measured up to 32.1 Gbits/sec.

• **Embedded test.** The days of probing test pads are coming to a close, especially for high-speed buses, because the practice can introduce anomalies into the signal. So where does that leave us? There is a growing interest in embedded test instruments, and the design-for-test movement is allowing nonintrusive embedded instruments to deliver the signal data that the receivers see. “In other words,” says Caffee, “soft access is provided to the hard data that signal-integrity engineers need.”

Embedded instruments have been used for years for chip-level characterization, verification, and test. But now, embedded instruments are being used to monitor and report data being received by the receiver. Caffee notes that the embedded instruments are accessed using standard technologies, such as the IEEE 1149.1 boundary-scan (JTAG) test-access port.

“JTAG provides access to an external software-based platform that can manage the embedded instruments in the system, as well as compile and analyze the test and measurement data they gather,” Caffee says (Figure 6).
Figure 6 An eye diagram like this one can be generated by a tool set for embedded instrumentation (courtesy Asset InterTech).

As system speed and complexity continue to rise, the way forward looks to be a combination of advanced measurement tools and techniques that work with customized simulation models. In the end, though, the path of least resistance for improving signal integrity looks to be an industry standby: good old-fashioned engineering ingenuity.

References

You can reach Janine Love, editor in chief of Test & Measurement World, at 1-973-864-7238 and janine.love@ubm.com.