Addressing signal electromigration (EM) in today’s complex digital designs


Abstract
Electromigration (EM) is a phenomenon that has been well researched and understood by the design community. At mature nodes, its impact on digital integrated circuits, particularly signal interconnects, has been minimal, making signal EM analysis and fixing an optional design step. At 28 nm and beyond, this is no longer the case. Interconnects are getting thinner, running longer and switching at gigahertz speeds - all of which amplify the effects of EM. Signal EM analysis and fixing is turning into a design requirement that must be met during place and route. This article discusses the importance of signal EM and ways to address it in today’s complex designs. It also highlights the EM capabilities in IC Compiler with results from Altera’s successful adoption of the solution for its 28-nm high performance IPs.

Electromigration 101   - A refresher
Electromigration (EM) is the gradual displacement of metal atoms in a semiconductor. It occurs when the current density through the conductor is high enough to cause the drift of metal ions (Fig 1).

EM decreases the reliability of integrated circuits (ICs). An EM failure at its worst manifests itself as either a void (open) or a hillock (short), which eventually leads to circuit malfunction (Fig 2).

Figure 1 : [Electromigration in a conductor], Source – Synopsys

Figure 2 : [EM failures - Void (Open) and Hillock (short)], Source – W.D. Nix et al. 1992
**Signal EM - Why it matters more than ever**

While EM and its impact on designs have long been understood, in mature technology nodes the effects were minimal and were not a big concern. Due to wider interconnects, lower operating speeds and smaller design sizes, manual methods or a conservative approach of oversizing wires for EM served as plausible solutions. However, at 28 nm and beyond, scaling trends in advanced technology nodes along with stringent and complex EM rules make designs more susceptible to EM – particularly on clock and data interconnects. As a result, signal EM and its effects can no longer be ignored.

**Advanced technology trends**

Metal widths are shrinking because of geometry scaling, resulting in thinner interconnects. Interconnect lengths are also increasing to meet the complex device integration demands. These thin and long interconnects are switching at gigahertz speeds due to the push for higher performance. When combined, these factors result in higher current densities, which amplify the effects of signal EM at advanced technology nodes.

A clear indication of this trend can be seen in the chart below that plots EM violations seen on a sample block across varying technology nodes and clock frequencies (see Fig 2). At 28 nm, there are significantly more EM violations on signal interconnects compared to those at 65 and 40 nm.

![Figure 3: Signal EM violation plot using sample block](https://via.placeholder.com/150)

**Growing EM rule complexity**

In order to reflect the effects of advanced technologies, EM rules have also become more complex. EM rules are foundry-provided limits that specify allowable current densities for every metal layer. In the past, the limits provided were primarily width and junction-temperature based (as shown in Fig 4).

<table>
<thead>
<tr>
<th>Width/Area</th>
<th>Temp</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>90</td>
</tr>
<tr>
<td>0.1</td>
<td>0.9</td>
</tr>
<tr>
<td>0.2</td>
<td>1.7</td>
</tr>
<tr>
<td>0.4</td>
<td>3.3</td>
</tr>
<tr>
<td>0.8</td>
<td>6.6</td>
</tr>
</tbody>
</table>

![Figure 4: Sample EM constraint table](https://via.placeholder.com/150)

At 28 nm and below, we are seeing the addition of more dependencies, such as interconnect length, via dimensions and delta temperatures (metal line temperature increase over junction temperature when current passes through it).
EM analysis is a complex task that requires a significant amount of data interpretation and is compute intensive. With an increasing number of interconnects exposed to EM effects, fixing techniques must be automatic, accurate, and timing and design-rule check (DRC) aware. A stand-alone post place and route step would not be ideal as it would be iterative, require user expertise and can adversely affect performance.

For today’s complex and challenging designs, the only way to effectively analyze and fix signal EM is to address it during P&R.

**Addressing signal EM during place & route**
The three main components of an optimal EM solution are – analysis, prevention and fixing.

- Analysis

  Accurate signal EM analysis relies on a wide spectrum of data that includes modeling, extraction, timing, switching activity and foundry EM constraints/limits. There are two main steps in EM analysis – effective current calculation and EM violation detection (Fig 5).

  Effective current, which includes computing peak, RMS (Root Mean Square) and average values, helps evaluate the cumulative EM effect on a conductor. The analysis engine needs to determine these current values for every routing segment and via in the design. With designs today operating under different modes and corners, these current values (effective current and EM limit) will vary based on the timing, voltage and temperature in every scenario. It is therefore critical to have an EM analysis engine that is multi-corner, multi-mode (MCMM) aware.

  ![Figure 5: Components of Signal EM Analysis](source: Synopsys)

  Once effective current values are determined, an EM violation is detected based on the current limits derived from the foundry EM constraints (Fig 6).
Prevention
Prevention can be implemented for signals that have an increased probability for EM violation. For instance, due to their high toggle rates and large drive cells, clock nets are more at risk for EM than data nets. Clock nets with special width and spacing rules (NDRs) derived from their driver cells can help minimize the impact of EM. When applied during clock tree synthesis and honored during route, these NDRs enable a correct by construction approach to minimize unnecessary perturbation on the clock nets during signal routing.

Fixing
EM fixing is a function of sizing wires, vias and cells in order to effectively reduce the current density through them. A comprehensive fixing solution much like analysis would also need to be MCMM-aware. Two commonly used EM fixing approaches are wire widening and cell sizing.

Wire widening
Widening wires help increase allowable current limits and is an effective way to reduce EM effect. This can be achieved by either applying NDRs on nets or just by sizing up the violating segments. The latter would be more suitable to designs that are prone to congestion.

Cell sizing
Using smaller driver cells can help slow down data transition, which in turn reduces current density and the impact of EM. This method is effective when there is sufficient timing margin.

In addition to providing a robust MCMM-aware analysis and fixing mechanism, an ideal solution should have certain key features to facilitate adoption. Providing seamless integration into a P&R flow would offer easy setup and quick turnaround time. Not all EM violations are automatically fixable, hence user control on techniques along with an intuitive GUI is needed for faster analysis and debug. Lastly, an EM solution within place and route is effective only when it is accurate and convergent, making correlation to industry-standard SPICE simulators a must.

IC Compiler EM solution - Ideal for today’s complex designs
IC Compiler place and route offers an integrated signal EM solution. It provides comprehensive MCMM-aware analysis and an automated EM fixing flow. Use of a consistent database provides fast turnaround times, and a powerful GUI aids analysis and debug of EM violations.

**Signal EM flow overview**

The IC Compiler EM Flow (Fig 7 below) reads in EM constraints from the vendor library (Synopsys plib or IEEE 1603 ALF format) along with switching activity information (SAIF / Tcl). There is a prevention flow for clock nets where user provided cell-based NDRs are applied during clock tree synthesis and honored during routing. The signal EM analysis and fixing flow is enabled via a single command and should be performed after route optimization on a timing /route DRC clean database. The automatic EM fixing flow in IC Compiler uses both route and cell-based techniques such as segment sizing on wires/vias, net based NDRs and timing- aware cell sizing. Additional flexibility is provided through user control to select a specific technique based on design characteristics to further minimize impact to timing/DRC.

![IC Compiler Signal EM Flow](image)

**Figure 7: [IC Compiler Signal EM Flow], Source: Synopsys**

Most importantly, IC Compiler’s EM analysis is well correlated to HSPICE, offering an accurate and convergent solution for today’s challenging designs.

**Altera’s experience using IC Compiler EM solution**
Group background
Located in Altera’s headquarters in San Jose, Calif., the physical design engineering team managed by James Deng supports multiple RTL front-end teams for netlist to GDSII support and helps define implementation methodology for their high-performance designs. The team was chartered with implementing all the RTL-based IP and subsystem in Altera’s first high-performance 28-nm FPGA (Stratix V). In order to ensure that the reliability of their device was not compromised, the team decided to perform signal EM analysis for the first time ever and chose to use IC Compiler.

Design details and challenges
The design targeted for signal EM analysis was a PCI IP, which had a hierarchical implementation with 11 sub blocks partitioned for IP re-use (Fig 8) operating at 500+ Mhz.

Since the programmable IP had many functional modes and complex clock structures, MCMM-aware EM analysis was a must. The high aspect ratio of certain blocks also made them prone to routing congestion, which meant a conservative approach to EM fixing was not viable.

Altera’s EM flow
To prevent excessive EM violations post route, Altera chose to use NDRs on clock nets during CTS and followed with IC Compiler’s signal EM analysis and fixing flow after routing. Different MCMM scenarios were created for EM analysis in order to achieve the most comprehensive coverage. The segment-based fixing approach in IC Compiler was selected due to the high routing congestion in the design.

Results
IC Compiler’s automatic signal EM flow was able to fix the majority of the violations with minimal DRC impact. Shown below (Fig 9) are results from two of the PCI IP blocks.
A few violations were left unfixed due to congestion and were later addressed manually by designers.

Altera also found IC Compiler’s GUI features very useful and intuitive to view the EM current density maps and understand the hot spots in the design (Fig 10).

Furthermore, the report files provided clear and detailed information, making it simpler for the first-time user to comprehend the data (Fig 11).

Altera successfully ran IC Compiler’s signal EM flow on all the blocks in their first 28-nm FPGA chip and has now deployed it as part of their production flow.

Altera’s Design Engineering Manager, James Deng had this to say based on their experience - “We found that IC Compiler’s signal EM flow provided an easy solution with clear reporting and automatic fixing methodology. The MCMM feature in Signal EM was very useful to us. It reduced the risk of merging scenarios ad avoided pessimistic/optimistic analysis. We recommend using IC Compiler to check and clean all signal EM violations before signoff”.

**Conclusion**

At 28 nm and beyond, geometry scaling and higher frequencies have made EM failures not just a possibility but a reality for every design. Signal EM analysis has become an integral part of physical
design methodology. As experienced by Altera, IC Compiler provides an easy-to-use, accurate and comprehensive EM solution that addresses the needs of today’s complex and challenging designs.

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James Deng is the physical design engineering manager at Altera. He is responsible for developing ASIC-style physical design solutions, and implementation of high performance digital IPs at cutting-edge technology node. He has over 16 years of experience in ASIC/SoC/FPGA semiconductor industry. Before joining Altera, he worked at Bay Microsystem on network processor (NPU) design and verification. He also worked at LSI Logic as senior ASIC design engineer developing advanced ASICs from RTL to GDS. James holds MSEE degree in VLSI circuit design and computer engineer area from Purdue University and a BE degree from Tsinghua University in China.

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