Designing low-power video image stabilization IP for FPGAs

Dr S. Parker, W. Cranwell, RF Engines - February 19, 2013

Image stabilization is an important capability for many electro-optic sensors, where an operator or user is required to view the output imagery. The technique can therefore enhance many practical viewing systems, spanning a very broad range of applications including those found in defense and security sectors.

Stabilization provides a means for reducing both image blur and unwanted frame-to-frame image shifts and rotations, thereby aiding image interpretation and reducing the operator's workload. For those systems that require the operator to locate or classify features within the video stream (typically recognition and identification), then a stabilized image stream will help improve the accuracy of these tasks.

There are a number of techniques for stabilizing an image which are either based on mechanical correction or image processing. Mechanical stabilization techniques include those that gyroscopically stabilize the whole camera system or use elements within the camera to effectively move the lens or detector array.

Mechanical stabilization techniques are well-established, although they can have a limited rate of response. Furthermore, they tend to be more expensive, consume more power and are physically larger and heavier. Mechanical stabilization techniques used within the camera housing are generally less expensive and are physically more compact. However, they can have performance limitations such as an inability to correct for roll, and may operate over a restricted range of unwanted camera movements. In addition, such integrated camera techniques are less well-established for infrared cameras and those cameras that use interchangeable lenses. Finally, it should be noted that mechanical stabilization corrects for movement associated with the camera, but does not correct for other effects such as atmospheric scintillation.
Digital video stabilization techniques provide image correction by using information from within the video-stream and this includes movements of the camera, any atmospheric effects, and movement within the scene itself. The approach offers a potentially significant performance gain with minimal impact on power, weight, and size. However, to realize these benefits, the stabilization algorithm complexity can be high, which translates into a high computational load. Although electronic stabilization can be achieved using a low-cost CPU architecture, the limited processing bandwidth restricts the maximum input image size and frame rate. Consequently, the capability of the stabilization algorithms has to be compromised to facilitate real-time operation. GPU architectures can be used to reduce the limitations associated with CPU-only devices and provide higher processing bandwidths that enable more complex processing. However, GPU implementations consume more power and often still need an additional system host for designs based on commercial-off-the-shelf products.

The approach taken by RFEL has been to specify a high-performance stabilization system that can readily support high input resolutions and frame rates, while maintaining low latency and power consumption. Also, the solution was required to be compatible with cameras that operate over different spectral bands, with support of multiple camera interfaces.

Physically, a flexible and compact hardware implementation was required that supports both stand-alone and networked applications. Furthermore, the stabilization solution should allow rapid integration into third-party hardware, including retro-fitting into in-service equipment.

To meet these challenging requirements, RFEL elected to base the implementation on the latest FPGA architectures which have embedded ARM processors. Compared with a GPU implementation, the primary drawback was the required engineering development time which is significantly higher when compared with a CPU / GPU software module implementation.

Fortunately, RFEL has been developing advanced signal and video processing modules for many years, which allowed substantial re-use of pre-existing functions and development tools. Initially, functional requirements were captured by liaising with major customers in the military and security sector.
The system was then designed and developed using RFEL’s proven methodology of floating and fixed-point modeling in Matlab that allows efficient performance testing, rapid debugging and substantially de-risks all aspects of system implementation.

A fundamental challenge in the development of any video processing product is the complexity and diversity of the imagery that must be processed by the product for the large range of applications. Experience has shown that the development of a video processing function, with testing confined to only a limited data set, can introduce significant program risk as discovery of ‘corner case problems’ late in the development may necessitate substantial rework. Consequently, RFEL performed a series of trials using various cameras and platforms, with imagery gathered at different times of the day and under various weather conditions. The data gathered was sufficiently diverse to give confidence that the stabilization design would be fit for purpose for land, maritime and airborne applications.

Page 3

Several contrasting approaches can be used for electronic image stabilization. The first, and most popular, is the use of prominent image features to generate frame-to-frame flow vectors. Typically, this approach involves feature detection and tracking of these features between frames. If the frame-to-frame movement is assumed to be low and high detection thresholds are used then the implementation can be relatively simple. However, performance and robustness when operating with diverse imagery can be poor.

![Figure 2: Stabilized image set. The rotation correction can be readily gauged from the edges of the image frame.](image)

In terms of the derived requirements, the RFEL stabilization function was specified to deliver a stable image under the most demanding of applications covering: driving aids for military vehicles, diverse airborne platforms, targeting systems and remote border security cameras. Furthermore, the algorithm design was required to stabilize images subjected to two-dimensional translation and rotation from both static and moving platforms. It is envisaged that the stabilization function will be used for supporting many different physical equipment installations. As such, the center of rotation could be within the camera or external to it and the stabilization algorithm must be able to cope with such installations. The stabilization function was required to provide real-time correction at frame-
rates of up to 150Hz for various imaging devices and for resolutions of up to 1080p including both daylight and infrared cameras. For example, a 1080p color camera operating at 8-bits and with a frame-rate of 60Hz, necessitates operation with an input data rate of about 1 Gbits/s. An FPGA-based hardware implementation provides the computational resources needed to process several gigabit/s input data rates with the selected spatial frequency stabilization method. However, even with the inherent processing power of an FPGA, the implementation has to be carefully tailored to satisfy the stringent latency and power consumption constraints. Given that the stabilization function is likely to be only one component of a larger processing suite, it was also necessary to minimize the number of gates and external memory accesses used.

The level of stabilization accuracy achieved under a very diverse and demanding range of evaluation test data was typically less than ± 1 pixels, even when subjected to random frame-to-frame displacements of up to ± 25 pixels in x and y directions and with a frame-to-frame rotational variation of up to ± 5°. The performance of the stabilization function is illustrated with figures 1 and 2, using a small number of frames from a daylight camera.

The performance of the stabilization design is shown using five consecutive frames from a sequence, when subjected to a random frame-to-frame rotation as large as ± 1° around the center of the image. The design has proven to be extremely flexible and can be used for both static and moving camera platforms. Although this capability can be delivered through an FPGA only implementation, further capability and performance can be achieved through additional software functions hosted on the ARM multicore processors embedded in the latest FPGAs.

The stabilization design was originally implemented on a development platform for Xilinx’s Zynq-7000 All Programmable SoC, which hosts an ARM Cortex-A9 MPCore dual core processor. This development board allowed early revisions of the design to be matured based upon target device resource and processing constraints. The processor was accelerated by exploiting existing RFEL’s IP Core components that reside in the fabric of the FPGA and have been optimized and tested over the last 10 years. A specific hardware design was also undertaken that provides the stabilization IP Core, together with other video processing functions, in a fully integrated custom hardware system-on-module. This module can interface with many different standards such as Analogue, CameraLink and GigE based protocols such as GigEVision.

RFEL’s video image stabilization processing capability is now available as an IP Core, optimized for FPGA. The fully integrated hardware system-on-module that incorporates the stabilization function will be available in the second quarter of 2013 and may be ruggedized to military standards. This stabilization system offers exemplary performance even when the camera is subjected to extreme unwanted shifts and rotations. When this capability is coupled with a low power and low latency implementation, the design becomes highly suited to military and security applications, as well as more demanding commercial applications. In addition, the IP Core can be readily integrated with existing processor hardware with negligible impact on size and weight.

About the author

Dr Steve Parker is Principal Digital Systems Engineer and Technical Project Lead at RF Engines Ltd – www.RFEL.com.

He can be reached at Steve.parker@rfel.com

Wayne Cranwell is Technical Sales Engineer and Project Manager at RF Engines Ltd.
He can be reached at Wayne.cranwell@rfel.com

Courtesy of EETimes Europe

Related posts

  - Implementing analog functions in rugged, rad-hard FPGAs
  - NATO experiences of modeling military embedded systems
  - Ruggedized interconnects support military computing platforms
  - Debug a microcontroller-to-FPGA interface from the FPGA side
  - Virtex-6 ups processing power to military embedded
  - Optimizing FPGAs for power: A full-frontal attack
  - Saving size, weight in avionics, military or space power distribution systems
  - How to mitigate military component supply issues
  - Mil-Aero top 10 'How-To' articles for 2012

For more technical information on military and aerospace engineering visit EE Times' Military Aerospace Designline.