Wide range input converters

Wide range input -48V to 5V converter

Often converters must accommodate a wide range of inputs. Telephone lines can vary over considerable tolerances. Figure 4.38’s circuit uses an LT1072 to supply a 5V output from a telecom
input. The raw telecom supply is nominally -48V but can vary from -40V to -60V. This range of voltages is acceptable to the VSW pin but protection is required for the VIN pin (VMAX = 60V). Q1 and the 30V Zener diode serve this purpose, dropping VIN’s voltage to acceptable levels under all line conditions.

**Figure 4.38 • Wide Range Input Converter**

Here the “top” of the inductor is at ground and the LT1072’s ground pin at -V. The feedback pin senses with respect to the ground pin, so a level shift is required from the 5V output. Q2 serves this purpose, introducing only -2mV/°C drift. This is normally not objectionable in a logic supply. It can be compensated with the optional appropriately scaled diode-resistor shown in Figure 4.38.

Frequency compensation uses an RC damper at the VC pin. The 68V Zener is a type designed to clamp and absorb excessive line transients which might otherwise damage the LT1072 (VSW maximum voltage is 75V).

Figure 4.39 shows operating waveforms at the VSW pin. Trace A is the voltage and Trace B the current. Switching is crisp, with well controlled waveforms. A higher current version of this circuit appears in LTC Application Note 25, “Switching Regulators For Poets.”
3.5V to 35VIN-5VOUT converter

Figure 4.40’s approach has an even wider input range. In this case it produces either a -5V or 5V output (shown in dashed lines). This circuit is an extension of Figure 4.11’s basic flyback topology. The coupled inductor allows the option for buck, boost, or buck-boost converters. This circuit can operate down to 3.5V for battery applications while accepting 35V inputs.

Figure 4.41 shows the operating waveforms for this circuit. During the VSW (Trace A) “on” time, current flows through the primary winding (Trace B). No current is transferred to the secondary because the catch diode, D1, is reverse biased. The energy is stored in the magnetic field. When the switch is turned “off” D1 forward biases and the energy is transferred to the secondary winding. Trace C is the voltage seen on the secondary and Trace D is the current flowing through it. This is not an ideal transformer so not all of the primary windings energy is coupled into the secondary. The energy left in the primary winding causes the overvoltage spikes seen on the VSW pin (Trace E).
This phenomenon is modeled by a leakage inductance term which is placed in series with the primary winding. When the switch is turned “off” current continues to flow in the inductor causing the snubber diode to conduct (Trace F).

![Waveform Diagram](image)

**Figure 4.41 • Waveforms for Wide Range Input Positive -5V Output Flyback Converter**

The snubber diode current falls to zero as the inductor loses its energy. The snubber network clamps the voltage spike. When the snubber diode current reaches zero, the VSW pin voltage settles to a potential related to the turns ratio, output voltage and input voltage.

The feedback pin senses with respect to ground, so Q1 through Q3 provides the level shift from the -5V output. Q1 introduces a -2mV/°C drift to the circuit. This effect can be compensated by a circuit similar to the one shown in Figure 4.38. Line regulation is degraded due to Q3’s output impedance. If this is a problem, an op amp must be used to perform the level shift (see AN19, Figure 29).

**Wide range input positive buck converter**

**Wide range input positive buck converter**

Figure 4.42 is another example of a positive buck converter. This is a simpler version compared to the synchronous switch buck, Figure 4.32. However, efficiency isn’t as high (see Figure 4.34). If the PMOS transistor is replaced with a Darlington PNP transistor (shown in dashed lines) efficiency decreases further.
Figure 4.43a shows the operating waveforms for this circuit. The pass transistor’s (Q1) drive scheme is similar to the one shown in Figure 4.32. During the VSW (Trace A) “on” time, the gate of the pass transistor is pulled down through D1. This forces Q1 to saturate. Trace B is the voltage seen on the drain of Q1 and Trace C is the current passing through Q1. The supply current flows through the inductor (Trace D) and into the load. During this time energy is being stored in the inductor. When voltage is applied to the inductor, current does not instantly rise. As the magnetic field builds up, the current builds. This is seen in the inductor current waveform (Trace D). When the VSW pin is “off,” Q2 is able to conduct and turns Q1 off. Current can no longer flow through Q1, instead D2 is conducting (Trace E). During this period some of the energy stored in the inductor will be transferred to the load. Current will be generated from the inductor as long as there is any energy in it. This can be seen in Figure 4.43a. This is known as continuous mode operation. If the inductor is completely discharged, no current will be generated (see Figure 4.43b). When this happens neither switch, Q1 or D2, is conducting. The inductor looks like a short and the voltage on the cathode of D2 will settle to the output voltage. These “boingies” can be seen in Trace B of Figure 4.43b. This is known as discontinuous mode operation. Higher input voltages can be handled with the gate-source Zener clamped by D2. The 400 milliwatt Zener’s current must be rescaled by adjusting the 50Ω value. Maximum gate-source voltage is 20V. The circuit will function up to 35VIN. At inputs beyond 35V all semiconductor breakdown voltages must be considered.
Buck-boost converter

The buck-boost topology is useful when the input voltage can either be higher or lower than the output. In this example, Figure 4.44, this is accomplished with a single inductor instead of a transformer, as in Figure 4.40 (optional). However, the input voltage range only extends down to 15V and can reach to 35V. If the maximum 1.25A switch current rating of the LT1072 is exceeded an LT1071 or LT1070 can be used instead. At high power levels package thermal characteristics should be considered.
The operation of the circuit is similar to the positive buck converter, Figure 4.42. The gate drive to the pass transistor is derived the same way except the gate-source voltage is clamped. Remember, the gate-source maximum voltage rating is specified at ±20V. Figure 4.45 shows the operating waveforms. When the VSW pin is “on” (Trace A), the pass transistor, Q1, is saturated. The gate voltage (Trace B) is clamped by the Zener diode. Trace C is the voltage on the drain of Q1 and Trace D is the current through it. This is where the similarities between the two circuits end. Notice the inductor is pulled to within a diode drop, D2 above ground, instead of being tied to the output (see Figure 4.42). In this case, the inductor has the input voltage applied across it, except for a Vbe and saturation losses. D4 is reverse biased and blocks the output capacitor from discharging into the VSW pin. When the VSW pin is “off” Q1 and D2 cease to conduct. Since the current in the inductor (Trace E) continues to flow, D3 and D4 are forward biased and the energy in the inductor is transferred into the load. Trace F is the current through D3. Also, D2 keeps Q1 from staying on if the circuit is operating in buck mode. D1, on the other hand, blocks current from flowing into the gate drive circuit when operating in boost mode.
Wide range switching pre-regulated linear regulator

In a sense, linear regulators can be considered extraordinarily wide range DC/DC converters. They do not face the dynamic problems switching regulators encounter under varying ranges of input and output. Excess energy is simply dissipated at heat. This elegantly simplistic energy management mechanism pays dearly in terms of efficiency and temperature rise. Figure 4.46 shows a way a linear regulator can more efficiently control high power under widely varying input and output conditions.
The regulator is placed within a switched-mode loop that servo-controls the voltage across the regulator. In this arrangement the regulator functions normally while the switched-mode control loop maintains the voltage across it at a minimal value, regardless of line, load or output setting changes. Although this approach is not quite as efficient as a classical switching regulator, it offers lower noise and the fast transient response of the linear regulator. The LT1083 functions in the conventional fashion, supplying a regulated output at 7.5A capacity. The remaining components form the switched-mode dissipation limiting control. This loop forces the potential across the LT1083 to equal the 1.8V value of VREF. The opto-isolator furnishes a convenient way to single end the differentially sensed voltage across the LT1083. When the input of the regulator (Trace A, Figure 4.47) decays far enough, the LT1011 output (Trace B) switches low, turning on Q1 (Q1 collector is Trace C). This allows current flow (Trace D) from the circuit input into the 10,000µF capacitor, raising the regulator’s input voltage.

![Figure 4.47 • Switching Pre-Regulated Linear Regulators Waveforms](image)

When the regulator input rises far enough, the comparator goes high, Q1 cuts off and the capacitor ceases charging. The MR1122 damps the flyback spike of the current limiting inductor. The 0.001µF-1M combination sets loop hysteresis at about 100mVP-P. This free-running oscillation control mode substantially reduces dissipation in the regulator, while preserving its performance. Despite changes in the input voltage, different regulated outputs or load shifts, the loop always ensures minimum dissipation in the regulator.

Figure 4.48 plots efficiency at various operating points. Junction losses and the loop enforced 1.8V across the LT1083 are relatively small at high output voltages, resulting in good efficiency. Low output voltages do not fare as well, but compare very favorably to the theoretical data for the LT1083 with no pre-regulator. At the higher theoretical dissipation levels the LT1083 will shut down, precluding practical operation.
Figure 4.48 • Efficiency vs Output Current for Figure 4.46 at Various Operating Points


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