Book review: An ASIC Low Power Primer

Brian Bailey - April 16, 2013

An ASIC Low Power Primer: Analysis, Techniques and Specification

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Perhaps you are an experienced designer, but you have just been told that you have to reduce the power consumption of the next ASIC by 50% and it has to run faster than the previous version with a bunch of new capabilities. What are you going to do? Perhaps the first thing is to obtain a copy of this book and it will guide you through all aspects of the knowledge you will need to understand your choices and set you off in the right direction - even perhaps a plan of how you are going to achieve the goal. Through standards such as the Liberty format for specifying cells to SAIF for specifying activity and CPF and UPF for specifying power intent, it covers all of the formats and languages that you will need to drive a design and implementation flow.

This book has been put together by Rakesh Chadha and J. Bhasker, both at eSilicon Corporation, a company that does contract chip design work. J. Bhasker concentrates in the area of hardware description languages and RTL synthesis. He has been chair of two working groups: IEEE 1076.6 VHDL Synthesis and IEEE 1364.1 Verilog Synthesis and was awarded the IEEE Computer Society Outstanding Contribution Award in 2005. He is an architect at eSilicon responsible for the timing of many complex designs. Rakesh Chadha is an experienced CAE and design professional. He was responsible for the timing and signal integrity for the Sematech project on Chip Parasitic Extraction and Signal Integrity Verification. He is Director of Design Technology at eSilicon Corporation and is responsible for complex SOC design methodology.

Chapter 1 - Introduction

This chapter talks about the reasons why power levels are increasing and various reasons why there is a growing need to reduce power consumption by all kinds of devices. Interestingly, it does not talk about ultra-low-power devices such as those that would rely on power scavenging.

Chapter 2 - Modeling of power in core logic
This chapter expands on some of the concepts introduced in chapter 1 – specifically where the power is consumed and the physics associated with static and dynamic power consumption and in turn the things that contribute towards each of these. It does try not to get buried too deeply in the physics. The chapter starts to use energy and power tables as a way to describe the various power drains. It starts showing how cells would be modeled using the Liberty modeling language.

**Chapter 3 - Modeling of power in IOs and macro blocks**

Almost all chips these days contain large amounts of memory and other common elements such as IO blocks, PLLs and SerDes. This chapter looks at them in more detail and some of the ways in which additional factors have to be taken into account.

**Chapter 4 - Power analysis in ASICs**

How often do signals switch? This is the primary factor that affects the amount of dynamic power a block consumes. Add that to leakage power and you obtain the total current draw. This chapter looks at various common elements of a chip such as gates, flip flops and memory cells. It discusses vectorless as well as calculations based on stimulus and the SAIF standard for specifying activity. I would like to have seen some examples of the time these techniques take and the correlation of results so that it would be easier to decide which techniques may be appropriate.

This chapter is to be excerpted. Part 1 is available [here](#). Check back next week for part 2

**Chapter 5 - Design Intent for Power Management**

There are many ways in which power can be managed in a design such as power gating and multiple voltage domains. Special circuitry is required at the boundaries and this chapter discusses where these are required. This is a large topic and I wish this chapter had gone into more detail.

This chapter is to be excerpted after chapter 4 has been completed. Check back each week for another piece of the book.

**Chapter 6 - Architectural Techniques for Low Power**

All design decisions affect power, some more so than others. This chapter looks at a few architectural techniques that can result in reducing power consumption such as variable frequency and dynamic voltage, power gating, memory access techniques.

**Chapter 7 - Low Power Implementation Techniques**

Even with a well architected design, there are further power savings to be made with the implementation and that is the focus of this chapter. Cell selection and sizing, clock gating and management of current rushes are some of the subjects tackled.

**Chapter 8 - UPF Power Specification**

The Unified Power Format (UPF) can be used to specify power directives throughout the flow and to drive simulation, synthesis and physical design. This chapter takes a look at the Accellera and IEEE specification.

**Chapter 9 - CPF Power Specification**

Another power specification language is the Common Power Format (CPF) defined by the Low
Power Coalition of Si2. This chapter looks at the major pieces of that language.

Appendix A - SAIF Syntax

The syntax for three types of SAIF (backward, forward and RTL forward) are provided.

Appendix B UPF Syntax

Overall impressions

The book provides lots of examples. It starts with small examples and builds up to architectural techniques that can be used to manage the power consumption in an ASIC. The downside of this is that those examples take up a lot of room in the book and for most of them having the complete listing is not really that useful.

Some level of knowledge about design and the ASIC process is assumed so the book is probably best for someone who has some experience but is perhaps just starting to take power reduction seriously. At the same time, I feel that a top-down flow may have been better suited for those looking at making changes in their design flows.

Obtaining the book

Springer provide a free preview of the book here

It is priced at $139 or $109 for the ebook.

It is also available from Amazon for a few dollars less

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