Editor’s Note: An update to this Design Idea appears in the June 2013 EDN.

The classical technique for demagnetizing the transformer in any forward converter is to implement a second winding bifilar with the primary winding to ensure continuous flow of the magnetizing current when the power switch (typically a power FET) turns off. Such a circuit generally limits or clamps the FET’s drain-to-source voltage to two times the dc supply-rail voltage. The same technique—using this recuperating winding—can be successfully implemented in a flyback topology to deal with the leakage-inductance problem.

Note that in any flyback converter, the flyback transformer (multiwinding inductor) is far from perfect; leakage inductance (primary to secondary) is as much as 5% of the magnetizing primary inductance. The leakage inductance ($L_{LK}$) is effectively in series with the power FET (drain connection). Complicating matters, the parasitic output capacitance of the FET ($C_{OSS}$) forms a series-resonant circuit with $L_{LK}$. When the FET turns off, very high overvoltage and ringing can occur. The higher the Q of the circuit, the higher the ringing voltage. This situation will likely cause significant EM interference and, due to the elevated FET drain voltage, lower the FET reliability.
Figure 1a A passive snubber is realized by adding a bifilar winding, $N_R$, and a diode, $D_3$, to a flyback transformer.

Figure 1a shows a flyback converter with such a recuperating winding added on a modified demonstration board (STMicroelectronics’ Viper17L). Some important considerations: Resistors $R_{s1}$ and $R_{s2}$ are sense resistors used for monitoring the currents; scope measurements for currents are measured directly across these resistors. The transformer ratios are the same as in the original transformer. The recuperating winding, $N_R$, is magnetically coupled tightly to only the primary winding, $N_P$, by making these two windings bifilar. Bifilar windings are made by simultaneously winding two wires side by side around the magnetic core, or bobbin; this approach maximizes coupling and tightly matches the parasitic capacitance and inductance. The coupling between the primary and the other windings is not as important.

Figure 1b Without any snubbers, the ringing on voltage (Channel 1, blue) and current (Channel 2, red) waveforms can be quite big.

In Figure 1b, it can be seen that without any clamping ($D_3$ disconnected), the voltage at the FET’s drain (IC1, pins 7 and 8) due to the ringing reaches 560V peak. The primary current is shown magnified in Figure 2a. At the moment the FET turns off, the primary current (magnetizing current) remains constant, charging the capacitance, $C_{OSS}$. This is indicated by the step waveform. The magnetizing current remains constant, as diode $D_i$ on the secondary side is still not conducting; this can be seen from the secondary current waveform in Figure 2b. The short period of time after the turn-off (when $D_i$ is not yet conducting) is the time when the series-resonance circuit’s $C_{OSS}$ is charged. Corresponding to the time when the FET’s drain voltage, $V_{DS}$, becomes high enough, $D_i$ becomes forward biased and the energy stored in the series-resonant tank circuit is released. The energy stored is a function of the resonant circuit’s Q factor and is surprisingly high.
In these results from the series tank circuit, there is ringing at the FET’s drain ($V_{DS}$, Channel 1, blue) after the primary current (Channel 2, red) charges $C_{OSS}$ following turn-off (a). $V_{DS}$ is again shown as Channel 1; the charging of $C_{OSS}$ delays the secondary current through $D_4$ (Channel 2) by just under 100 nsec (b). The bifilar winding, $N_p$, steers the primary current (Channel 2) back to the power rail and clamps the switch voltage (Channel 1) (c). The leakage flux fights the current transfer; the secondary current (Channel 2) rises to an equilibrium peak value until the leakage energy is fully recuperated (d).

When the recuperating winding, $N_r$, and diode $D_3$ are connected to the power-supply rail, a completely different process is observed. The recuperating winding simply bypasses the parasitic $C_{OSS}$, steering the accumulated leakage energy back to the supply rail. In Figure 2c, it should be noted that the negative surge of the primary current (Channel 2) is actually the current flowing from the recuperating winding. The secondary diode, $D_4$, is forward biased immediately (Figure 2d); as the secondary current (Channel 2) rises to the steady-state peak value, the primary current diminishes to zero. As $N_p = N_r$, this assures limiting of the $V_{DSS}$ to two times $V_{DC}$.

Eliminating the excessive ringing by leakage-energy recuperation is clearly an advantage as all other passive RCD snubber techniques dissipate this energy and thus lower the efficiency of the converter. Limiting the maximum $V_{DS}$ to two times $V_{DC}$ is acceptable bearing in mind that most monolithic embedded converters incorporate high-voltage power FETs. (STMicroelectronics’ Viper17, for example, has an impressive 800V rugged power section.) Bifilar windings are readily available from most of the transformer vendors, or, for in-house production, a Multifilar magnet wire can be used to make these windings.

**References**