GNSS Receiver Frequency Reference for Successful Satellite Navigation

Desmond Wong - May 06, 2013

Title-4
The market acclaimed SE880 3D SiP GNSS receiver – world’s smallest and most technologically advanced GNSS receiver module was designed to relieve the design engineer from the burden of running to the chipset maker’s reference design and spending the next 12 months trying to arrive at a working GNSS system. So why is it that even as mighty in all relevant dimensions such as sensitivity and power consumption as is the miniature 4.7mm x 4.7mm receiver, it still requires a customer supplied 32KHz crystal and temperature-compensated crystal oscillator (TCXO)? This article delves into the vast world of crystal and TCXO specifications and guides design engineers and product managers through XTAL/TCXO pairing methodology and criteria fundamental to the creation of a GNSS solution that will work - 100% - well for their application and environments.

Fundamentals
Global navigation satellite system or GNSS receivers on or near the Earth’s surface use ranging signals transmitted from satellites to determine position and synchronize time. A frequency reference is the cornerstone of the technology’s accurate timing - from the atomic clocks onboard the satellites to the oscillators operating within the GNSS receivers. In fact, in designing GNSS receivers two are needed. Moreover, selecting and designing-in these components are critical elements to the performance of the receiver.

Primary oscillators are predominantly mass-produced TCXOs which provide the master frequency reference for satellite signal detection and measurements. The secondary oscillator is typically a 32KHz tuning fork quartz crystal with temperature stability of ±200ppm from -40°C to 85°C. This secondary oscillator is used to direct a real-time-clock (RTC) counter during “power saving” and “hibernate” modes. Upon exit from these modes RTC data supplied to the DSP helps regenerate system time reducing system initialization time.

Requirements for this crystal are much less stringent than for the TCXO as long as it can be kept away from heat-generating sources. A major consideration factor is the trade-off between size and cost. The smaller the crystal’s package, the higher is its cost. Due to increasingly constraining real estate and complexity in PCB, layouts most GNSS receivers in the market are designed with ultra-small (high-cost) on-board crystals to reduce the solution size to 100mm2 or less.

One way of achieving a sub-100mm2 footprint is, of course, to start with a small receiver SiP. Figure 1 (Right) shows how the use of a small GPS SiP (the Jupiter SE880 is shown here) plus a very low cost and widely available 1.5mm x 6.7mm crystal achieves a design of less than 50 mm2. The footprint can be further reduced to less than 40 mm2 (See Figure 1 left) if necessary with the selection of a smaller crystal package. Having the crystal external to the GPS SiP allows the final
complete design to easily fit different footprint constraints just by varying the selection of crystal package. This makes it possible to achieve ultra small solution footprints at a much-reduced cost.

Figure 1. Small total footprint achieved with a standard 32KHz tuning fork crystal

The Master Oscillator Requirement

Many ready-to-run GNSS modules are built with an on-board TCXO encapsulated under a metal lid. For reasons beyond the scope of this article (related to the spread-spectrum characteristics of CDMA and FDMA), the metal lid neither reduces electromagnetic interference nor increases sensitivity of GNSS receivers. Indeed, if the design doesn’t comply with the characteristics of the TCXO, the metal lid can in fact have an adverse effect on system performance. Ultra-small 1.6mm x 2.0mm TCXO packages are readily available and frequently used to address space constraints and complexity in PCB layouts, significantly increasing system cost while neither improving performance nor providing a versatile solution for different application environments.

TCXO stability is crucial for achieving good GNSS accuracy. GNSS TCXO manufacturers often guarantee that frequency stability can be maintained at ±0.5ppm over the specified operating temperature range. Table 1 shows a comparison of published specs for five commonly available brands of GNSS TCXOs. All exhibit similar phase noise with the same frequency stability across the operating temperature range. The better the phase noise, the higher the margin to provide reliable tracking performance at weak signals.

<table>
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<th>Vendor B</th>
<th>Vendor C</th>
<th>Vendor D</th>
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Table 1. Phase noise comparison of GNSS TCXOs at 16.369MHz reference frequency

However, achieving this good (specified) stability is contingent on a sound TCXO implementation. This needs to be done with good system design and engineering quality so as not to expose the TCXO to high rates of temperature change and voltage supply noise. In traditional designs, these two factors are hard to achieve as complex PCB routing and size requirements prevent application of adequate heat sinking and voltage supply filtering.

Figure 2 shows the voltage supply noise measured at the TCXO’s Vcc rail in a popular GNSS receiver module. Here the peak-to-peak Vcc ripple supplied to the TCXO is high at approximately 80mVp-p, against a common specification of less than 50mVp-p. This noise level will sensibly limit the choice of TCXO and require that extensive testing be conducted to verify the TCXO’s performance under this noisy Vcc supply.

Figure 2. Noisy Vcc going into TCXO of a popular GNSS receiver module

In contrast, Figure 3 shows how a better-engineered GNSS SiP (SE880 shown) provides a very clean Vcc with approximately 40mVp-p of noise. This power supply performance can easily meet requirement from most GNSS TCXOs available in the market today.

Figure 3. SE880 shows a cleaner Vcc meeting most TCXOs’ noise specs

The greatest factor to influence TCXO stability is temperature. Even a minor thermal disturbance can cause the TCXO frequency to drift and jump in the short term. Common limits for frequency drift and jump in GNSS receivers are 40 to 500 ppb in the first few seconds of power up and then five ppb per second thereafter.
Figure 4 (left) illustrates the effect on GNSS signal detection with a stable reference frequency. The graph on the right illustrates the case in which the reference frequency is drifting during integration of the signal processing. The correlation peak (code phase) moves during the integration period and results in increased probability of missed detection, acquisition failure rate and position errors, where signals are attenuated 10-30 dB from ideal open sky conditions or in urban canyons.

**Figure 4.** Correlation peak with stable reference frequency vs. drifting reference frequency

Figure 5 shows the GNSS accuracy when the TCXO exhibits reduced (desired) frequency drift and Figure 6 shows inferior GNSS accuracy when the TCXO is implemented with traditional design and technology.

**Figure 5.** GNSS Accuracy with enhanced TCXO implementation

**Figure 6.** GNSS accuracy is much reduced under traditional TCXO implementation

A Successful Frequency Reference Implementation
In a GNSS receiver with metal lid encapsulation, the biggest heat-generating source is the GNSS chip inside. Ideally, the TCXO should be kept as far away as possible from the GNSS chip and insulated from other high frequency traces and components that undergo large, sudden changes in current. However, with limited routing space inside a traditional module, the problem is not simply that heat sinking isn’t implemented properly for the GNSS chip, but that the TCXO is also packed closely inside. Further, vendors often recommend that the TCXO be well connected to the ground plane under the assumption that the TCXO’s ground is thermally stable.

Figure 7 shows the problem with traditional integration technology where space constraints eliminate the possibility for effective heat sinking around the GNSS chip (shared ground plane outlined in red). Complicating matters further the TCXO’s ground plane is connected to the heat generating ground plane right next to the heat source. Copper is highly effective transferring heat as it is 1,400 times faster than the FR4 substrate.

The solution for achieving thermal compliance for any GNSS TCXO is to provide a large and effective heat sink directly under and around the GNSS chip. Figure 8 reveals how that is viable where the heat sink and thermal compliance can be easily implemented in a low cost two-layer PCB. A large via hole is made underneath the GNSS chip (SE880 shown here) to establish a continuous copper path in the direction of heat flow. Due to the low thermal conductivity of the FR-4, the large via hole dominates the heat transfer away from the SE880 to the large layer-2 ground plane, yet not to the adjacent TCXO. The TCXO’s ground is on layer-1 and thermally insulated from that of the GNSS chip. This method allows the TCXO to be placed close to the GNSS chip while providing for thermal stability and clean grounding effect for both components.

**Figure 7. Traditional implementation - TCXO ground plane connected to the heat-generating source directly and right next to it**

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Figure 8. Enhanced TCXO implementation - a large via hole dominates heat transfer to layer-2; TCXO ground is clean and thermally stable

Figure 9 shows in a comparison of mean time to first fix (TTFF), how a system implemented with the enhanced design technique described above can acquire satellites 200 seconds faster than traditional design. In addition, Figure 10 shows the setting for the system used in the evaluation of this design: an indoor location inside a building in downtown Tokyo, Japan.

Figure 9. Enhanced design acquires satellites over 200s faster than traditional at a signal strength of -148 dBm
Summary
In the effort to select a well performing crystal and stabilize performance of the critical TCXO, there are design-strategies, which can help enhance system performance and allow the use of lower cost components. Additionally the application of novel GNSS 3D-SiP receivers such as the SE880 can reduce architecture complexity and make it easier for system developers to maintain healthier performance and design margins. And in the end, integrators have more freedom to innovate, increase engineering efficiency and reduce costs.

More about Desmond C. Wong

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