Ensure FinFET defect coverage with cell-aware test

Stephen Pateras - May 06, 2013

The size and performance advantages of FinFETs are leading to a general industry adoption of these 3D transistors at the more advanced technology nodes. These complex transistors, however, exacerbate the existing concerns over quality and reliability at 16nm and below. While there has already been a lot of research into the types of defects that are likely to occur within FinFETs, understanding and characterizing these defect mechanisms is only the first step. More critical, perhaps, is developing a methodology for generating test patterns that efficiently target these new defects. It turns out that this can be accomplished using the recently developed cell-aware test approach.

Cell-Aware Test

The process of generating test patterns for digital circuits, typically referred to as automatic test pattern generation (ATPG), has been in use for decades. The approach is based on modeling circuit defects to a level of abstraction that enables a computationally efficient test-pattern generation process. For years, the simple stuck-at fault model was used. As circuits grew in performance and complexity, new fault models were gradually introduced and adopted to account for the growing probability of more complex defect types. Some of the most common of these include transition, bridging, open, and small-delay faults.

As the industry moves to increasingly smaller geometries, we have discovered that all of these fault models and associated test patterns are becoming less effective for ensuring desired quality levels. The reason for this is that all of the existing fault models only consider faults on cell inputs and outputs, and on the interconnect lines between these cells. In other words, only faults abstracted to the netlist level have been explicitly considered. It turns out, however, that a growing number of defects occur within the cell structures. TSMC has stated, “...for 90nm and beyond, a significant number of manufacturing defects and systematic yield limiters lie inside library cells.” With more recent fabrication technologies, the population of defects occurring within cells is significant, perhaps amounting to roughly 50% of all defects.

A new methodology that targets defects within cells was recently developed to address this coverage gap. This cell-aware test approach targets specific shorts and opens internal to each cell. Each cell is modeled at the transistor level, and analog simulations are performed to characterize the effects of these potential short and open defects. Based on the analog simulation results, a cell-aware model is created that directs ATPG to generate patterns targeting these internal cell defects.

The first step in the cell-aware methodology is to characterize each cell in a technology library. The flow is illustrated in Figure 1. The transistor layout for each cell, typically in GDSII format, is required as a starting point. An extraction tool, such as Calibre xRC, is used to extract a transistor-level analog netlist, including parasitic capacitors and resistors, which are used to identify the
location of possible bridge and open defects, respectively. To model a potential cell internal bridge, then, the parasitic capacitor is replaced by a resistor model. Opens occur when there is a gap in a connection. In this case, a parasitic resistor that describes connectivity is replaced by a high-impedance resistor.

Figure 1: The cell-aware library characterization flow

Analog simulation is then performed to generate the cell-aware model. The analog simulation process iteratively modifies each parasitic element in the netlist, performs the simulation, and compares the results to the fault-free analog simulation to conclude if the inserted defect is detected or not. Defects are determined as “detected” when the cell’s output voltage deviates from the “good circuit” voltage by a specified percentage (typically 50%). However, not all bridge or open defects are detected by a static change in the output voltage. Some may result in a delay in the output voltage swing. For these defects, a dual-cycle analog fault simulation is performed at-speed in order to detect even small delays.

The final process in cell-aware characterization is to convert the list of input combinations into a set of the necessary input values for each fault within each cell. Because this fault information is defined at the cell inputs as logic values, it is basically a logic fault model representation of the analog defect simulation. This set of stimulus for each cell represents the cell-aware fault model file for ATPG.

Within this file, a simulated defect (now a fault) can have one or more input combinations. An example is shown in Figure 2. For this example fault ‘my_stuck_01’, ATPG will try to find any of the three input combinations when targeting this fault in a design. If any one of the combinations can be applied to an instance of the cell and the fault effect can be propagated to an observation point, then the fault is marked as detected for this instance; the other combinations are no longer necessary.

```plaintext
udfndef1.0 {
  udfndef"my_stuck_at" {
    cell "XDR2" {
      Fault "my_stuck_01" {
        Test { StaticFault "Z" = 0; Condition "A" = 0; Condition "B" = 1; }
        Test { StaticFault "Z" = 0; Condition "A" = 1; Condition "B" = 0; }
        Test { StaticFault "Z" = 1; Condition "A" = 0; Condition "B" = 0; }
      }
    }
  }
}
```

Figure 2: An example of a cell-aware fault model (shown above)

Because the cell characterization process is performed for all cells within a technology library, any design using that technology can read in the same cell-aware fault model file. Characterization only needs to occur once, and can then be applied to any design on that technology node. Modeling FinFET defects
Modeling FinFET defects
The cell-aware methodology is well suited for addressing defect mechanisms specific to FinFET. Consider a FinFET transistor with three fins, as illustrated in Figure 3. Recent research suggests that two defects types should be considered for such transistors: leakage defects that force the transistor partially or completely on, and drive-strength defects that force the transistor partially or completely off.

The leakage defects can be analyzed by placing a resistor across the gates (from drain to source) of each of the transistor’s three fins as shown in Figure 4. During the cell-aware characterization process, analog simulation is performed with varying resistive values for all resistors for all FinFETs in a given library cell. Exhaustive analog simulation must be performed for both single-cycle and dual-cycle tests, as many of these resistive defects will only result in small extra delays to the transistor’s response and, hence, to the output of the cell (see Figure 4).
The drive-strength defects can be analyzed by placing a resistor between the drain and each of the fin’s gates and between the source and the fin’s gates as shown in Figure 5. As with the leakage defects, analog simulation is performed with varying resistive values for each of the resistors. Once again, both single and dual cycle tests must be simulated to detect delay-related effects.

![Figure 5: Drive-strength defect simulation](image)

Any additional defect types that are discovered and are relevant to FinFETs can be handled in a similar fashion. The generic approach to analog defect simulation used by the cell-aware methodology makes this straightforward.

**Conclusion**
The cell-aware test approach has already proven to be very effective in increasing chip quality levels at various technology nodes from 350nm down to 20nm. This generalized approach to internal cell defect coverage is also fully capable of targeting new FinFET defect mechanisms and should prove indispensable in ensuring necessary quality in upcoming FinFET based designs.

**About Stephen Pateras**
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