Comparator-based buffer using a VVCCS

Seyyed Hossein Pishgar, Alihossein Sepahvand, Omid Hashemipour - June 14, 2013

Editor's note: PhD candidate, Seyyed Hossein Pishgar approached me with this paper, which I believe has some unique and creative circuitry and architectures. I have seen comparator-based buffers with resistive error correction out there in the past which enhance the driving capabilities of high-gain amplifiers to drive switched capacitor loads like those in an ADC front end. The error correction scheme uses a resistor in series with the charging path and a correction phase to reduce overshoot at the amplifier output.

In the following paper, Pishgar and his colleagues from the Microelectronics Lab and the Electrical/Computer Engineering Dept. at Shahid Beheshti University in Iran, demonstrate a comparator-based buffer circuit using a variable voltage-controlled current source that tames the amplifier overshoot tendencies. This seems to be a novel way to create such an amplifier to drive a switched capacitor load. The good news is that a comparator-based buffer will typically be a lower power solution than an op amp. The bad news is the tendency of the comparator-based buffer is overshoot. These students show a means to deal with this overshoot problem by means of a variable voltage controlled current source (VVCCS).

Here is that paper in its entirety.

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High precision comparator-based buffer using variable voltage controlled current source

Abstract. In this paper a new comparator-based buffer circuit which utilizes a variable voltage controlled current source (VVCCS) is presented. Application of a tractable current source results in an accurate performance which reduces both, the overshoot error at the output node and the variations of the overshoot error to the output voltage level. Simulations with 0.18μm CMOS technology verifies this method and estimates 616μw total power consumption for the proposed circuit.
Introduction

Nowadays, reducing the battery consumption is one of the priorities of circuit designers. Recently, a new kind of comparator based switched-capacitor circuit is presented [1]. It replaces the operational amplifiers, which stand for the biggest share of power consumption with a comparator, switches, current sources and logic control gates. While the op-amp based circuits force the input nodes to create the virtual ground, whereas, the comparator-based circuits realize the virtual ground condition. Nonetheless, these comparator-based circuits suffer from overshoot error. The overshoot error is basically the effect of the comparator finite delay, the current sources response time and logic control inherent latency. To handle this drawback, a fine current source is used to reduce the overshoot error. In [2], the comparator-based switched-capacitor is applied in a buffer circuit and it proposes a different approach regarding the overshoot error reduction. In order to compensate fine current source loss, switches and error correction resistor are used (Fig. 1(a)). Nevertheless, the buffer still suffers from significant overshoot error and also, variations of the overshoot error to the output voltage level.

In this paper, a new idea, to reduce both the overshoot error and the non-linearity of the overshoot error to the output, is applied to comparator-based buffers.

Proposed comparator-based buffer

The building block of the proposed buffer and the clock timing diagrams are depicted in Fig. 1(b) and (c), respectively. A dual-output comparator has been used to control the variable voltage controlled current source. In the preset phase, the output voltage is held to the lowest voltage of the circuit. Though the output is less than the input, the outputs of the comparator turn the current source on. The load capacitor is charged up and \( V_{\text{out}} \) is increased. In start of the \( \phi_1 \) phase, \( E_1 \) and \( E_2 \) are zero. Therefore, the maximum value of the current source flows through the circuit. As \( V_{\text{out}} \) is going up, \( E_1 \) is increased proportionally. Gradually, the current value of the VVCCS is reduced, so the output ramp is decreased.

Given, the \( E_2 \) can be Low or High. When \( V_{\text{out}} \) is crossing the input voltage level, \( E_2 \) is set High and the load capacitor no longer is charged. The effect of inherent delay of the circuit is reduced by using of VVCCS, so a negligible amount of the overshoot error is created at the output voltage. The overshoot error can be further decreased with high resolution comparators which compromise power consumption.
Variable voltage controlled current source

A customized variable voltage controlled current source [3] used in the proposed circuit is shown in Fig. 2(a). When \( E_1 \) and \( E_2 \) are at their lowest points, the maximum value of the output current is flowed through the output. When \( E_1 \) is increased, the current of \( M_2 \) and \( M_4 \) and so \( I_{out} \) is decreased. Finally, when \( E_2 \) is set High, \( M_5 \) is turned off.

Customized comparator

The used voltage comparator in the proposed comparator-based buffer is shown in Fig. 2(b) [4]. In order to increase the gain of the comparator, the post-amplifier stage differs from [4] in that it uses an nmos input amplifier. Furthermore, in this comparator the signal \( E_1 \) is driven from the drain of \( M_2 \) which clearly represents the changes of the signal \( V_{in} \), while the signal \( E_2 \) has only two states. There are three main blocks in this comparator; pre-amplifier stage which is constituted of \( M_1 \) and \( M_2 \), decision making stage which includes \( M_3 \)-\( M_6 \) and the rest of the circuit makes the post-amplifier stage. The first stage is just an elementary differential n-channel amplifier with active load from the second stage. Decision making process in the second stage goes as follow: first consider a situation when \( V_{in} \) is lower than \( V_{ref} \). In this state, \( M_4 \) is on and \( M_3 \) goes off. Hence, all the bias current passes via \( M_4 \) and \( M_6 \). In this case, \( E_1 \) and \( E_2 \) are at their lowest point. As \( V_{in} \) increases and approaches \( V_{ref} \), currents in \( M_4 \) and \( M_6 \) starts to decrease and hence \( E_1 \) rises gradually proportionally from ground to \( V_{in} \), while \( E_2 \) still is zero. When \( V_{in} \) crosses the \( V_{ref} \) level, the bias current flows through \( M_3 \) and \( M_5 \). Now, \( E_1 \) rises to high state fast, using regenerative properties of decision making stage. Finally, the post-amplifier stage is used to enhance the resolution of the comparator.
Simulation results

In order to verify the accuracy of the proposed comparator-based buffer, the circuit is simulated in HSPICE environment with 0.18μm standard CMOS process with 1.8V supply voltage. The common mode voltage, amplitude and the frequency of the sinusoidal input are assumed 0.9V, 0.2V and 10KHz, respectively. The circuit is clocked at 1MHz and the load is a 1pf capacitor. The input, output, E₁ and E₂ waveforms of the proposed circuit are shown in Fig. 3 Signals E₁ and E₂ and V_{out}. As it is shown the V_{out} voltage is increased with a high slope ramp when V_{out} is far below V_{in}. When V_{out} is closed the V_{in} voltage level, the output ramp slope is reduced. The E₁ signal should track the gradual increment of the output signal of the comparator. Also, the state of E₂ signal is triggered when V_{out} passes the V_{in} voltage level.

Various input voltage levels are applied to the proposed circuit and the outcome is outlined in Table 1. These findings are measured as the signal E₂ goes high.
### Table 1. The overshoot error versus the input voltage level and comparison with the results of the previous comparator-based buffers.

<table>
<thead>
<tr>
<th>Vin(V)</th>
<th>Overshoot(mV)</th>
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<tbody>
<tr>
<td></td>
<td>This Work</td>
</tr>
<tr>
<td>1.1</td>
<td>0.31</td>
</tr>
<tr>
<td>1.0</td>
<td>0.35</td>
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<tr>
<td>0.9</td>
<td>0.46</td>
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<tr>
<td>0.7</td>
<td>0.34</td>
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<tr>
<td>0.6</td>
<td>-</td>
</tr>
<tr>
<td>0.5</td>
<td>-</td>
</tr>
<tr>
<td>0.4</td>
<td>-</td>
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</tbody>
</table>

**Conclusion**

A new model for the typical comparator-based buffer was presented. In order to minimize the overshoot error, a variable voltage controlled current source is applied and a customized comparator with two outputs is employed. The better performance of the proposed circuit is revealed by comparing with the previous state of arts. Simulation results were handled in HSPICE environment with 0.18μm standard CMOS process. The power consumption of the proposed buffer is estimated to be 616μw.

**REFERENCES**


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