Introduction

Modern systems-on-chips (SoCs) are typically implemented in the most advanced process nodes available to take advantage of the smaller and faster properties of that process. This trend has allowed SoC architects to effectively address end users' expectations that each new product generation will offer higher functionality and performance, lower power and, hopefully, lower cost.

Increasingly, SoCs that follow this trend are at the center of mobile communications and wireless connectivity applications in smartphones or tablets, as well as other multimedia applications in the home such as digital TVs and set-top-boxes. The SoCs digitally process modulated analog signals that can be the output of wireless radios, wireline transceivers, or sensors. These signals must be accurately digitized for internal processing in the SoC by the analog-to-digital converters (ADCs) that are, therefore, an essential component in SoCs.

According to Moore's Law, SoC density is expected to increase by 1.5X-2X in every new process generation, and power consumption must reduce by the same factor. This scaling comes naturally in digital circuits that basically consist of interconnected switches. However, analog components cannot immediately take advantage of feature size reductions. In fact, dynamic range and accuracy requirements limit area and power consumption irrespective of process improvements. To achieve scaling factors similar to digital circuits, analog circuits must exploit the higher speed and processing power made available by Moore’s Law scaling. For example, more compact analog blocks can perform the same functions of more complex ones by relying on digital compensation, calibration, and higher processing speed, leading to the concept of digitally enabled analog circuits.

This whitepaper elaborates on how ADCs can work with Moore’s Law to move with the power and area scaling trends that are common for digital circuits. It will:

- Compare the main ADC architectures and conclude that the Successive-Approximation Register (SAR) based ADC is very well positioned as the architecture of choice for medium- and high-speed ADCs in modern SoCs, especially in 28-nm processes and beyond.
- Describe implementations of the SAR ADC architecture that reduce power consumption and area usage dramatically, enabling SoC designers to successfully integrate these analog components in their next SoCs.
- Present the most recent Synopsys SAR-based ADC family for 28-nm and explain how they fully benefit from the characteristics of the advanced process nodes, thus yielding analog IP that adheres to the area and power scaling paradigms of the digital circuitry, with improved overall analog performance.
ADC Architectures

The main function of the ADC consists in generating a binary coded representation of the analog input signal. For example, a 10-bit resolution ADC with a reference voltage of 1V (relative to ground) is able to represent any input level between 0 and 1V by one of its 1024 \(2^{10}\) codes, with a resolution step of about 0.975mV.

Several different architectures, from ramping to parallel, have been used to implement this function. Their particular characteristics make them more suitable to address different resolution and sampling rate ranges. Traditionally, they are distributed as shown in Figure 1.

![Figure 1: Traditional areas of application of ADC architectures](image)

Each ADC architecture brings its own merits:
- Flash, or Parallel, architectures perform the data conversion in a single step, making them very fast. However they can be power hungry and their analog circuit count increases exponentially with the number of bits, so its usage is typically limited to low-resolution applications.
- Ramping architectures perform the conversion by measuring the amount of time it takes for a slow reference ramp to cross the input signal level. These converters can achieve very high resolution but are limited to very slow applications.
- Sigma-delta architectures use high oversampling rates and noise shaping techniques to create a high-speed bit stream whose density accurately represents the input signal. The digital representation of the input signal results from the accumulation of a long period of the bit-stream, yielding a relatively slow effective conversion rate. This characteristic makes them useful especially for high-resolution, low- to moderate-speed applications.
- Pipeline architectures make use of cascaded conversion stages, each performing a very fast low resolution conversion, followed by the calculation of the residue that is provided to the next stage for further processing. The fact that the conversion is achieved with multiple, similar, successive steps yields a modular architecture. This architecture can deliver medium resolution (10- to 12-bit) and high speed (up to 100’s of MSPS). However, latency can be high due to the sequential nature of the conversion.
- The SAR architecture digitizes the input signal step-by-step by running a successive approximation algorithm and determining each bit one by one until the complete conversion is finalized. This architecture reuses the same hardware for each step; therefore, it requires a high clock rate to complete the conversion before the next sampling instant. For example, a 11x clock rate may be used for a 10-bit ADC. Consequently, this architecture has traditionally been limited to low-speed, medium- to high-resolution applications.
Table 1 summarizes the key tradeoffs of the ADC implementations shown in Figure 1.

<table>
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<tr>
<th>Architecture</th>
<th>Latency</th>
<th>Speed</th>
<th>Resolution</th>
<th>Area and power consumption</th>
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<tr>
<td>Flash</td>
<td>Low</td>
<td>Very high</td>
<td>Low</td>
<td>High</td>
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<tr>
<td>Ramping</td>
<td>High</td>
<td>Very slow</td>
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<td>Sigma-delta</td>
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<td>SAR</td>
<td>Low</td>
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Table 1: Tradeoffs of ADC architectures

**SAR ADC Architecture for High-speed and Low-power at 28-nm and Below**

Given the high speed and processing power achieved with modern process nodes, at 28-nm and below, the SAR ADC is becoming very competitive and thus the subject of deeper scrutiny. In fact, the number of publications on SAR-based ADCs continues to grow[1]. The architecture is very efficient, even where pipeline or parallel ADCs had been the norm[1].

One interesting aspect of the SAR architecture is its inherent simplicity. Contrary to established architectures such as the pipeline, the SAR-based architecture does not rely on multiple stages (each containing large gain amplifiers), or on the detailed analog characteristics of the process to achieve performance. Rather it is a single-stage comparator, which is inherently very compact and low power. Furthermore, it is mostly insensitive to the analog characteristics of the process.

**SAR architecture basics**

Figure 2 shows the basic block diagram of a SAR ADC including a sample-and-hold (S&H), a comparator, a digital-to-analog converter (DAC) and a logic block (SAR). The input signal ($V_{in}$) is stored on the sample-and-hold and is successively compared to the output of the DAC, whose input codes are set by a logic block depending on the result of the previous comparisons.

The logic block controls the search for the code that represents the input signal level. It uses an algorithm invented 500 years ago, when people needed to measure the weight of an object in the minimum amount of operations. In 1556, the mathematician Niccolò Tartaglia suggested using a binary series of weights. Today, this algorithm is called Successive-Approximations and starts by comparing the stored input signal with the mid-range of the ADC, by asserting the Most Significant Bit (MSB). The output of the comparator will tell if the input signal is on the upper or lower half of the range and set the MSB accordingly. Next, the second MSB is asserted allowing to further test on which half of the already resolved range the input signal is; this process continues until the Least Significant Bit (LSB) is resolved. The process takes N steps for a N-bit ADC.
The beauty of this architecture is that no power hungry precision amplifier is required, as it employs only blocks that can be designed with zero static power consumption. Moreover, the sample-and-hold can be merged with the DAC by the use of switched capacitors, further reducing the area and eliminating interfaces. Figure 3 shows a simplified schematic of a SAR ADC for 6-bit resolution. The input signal (V_{IN}), is initially sampled on the top-plate of the capacitor array. Next, with the top-plate now floating and storing the input signal, the individual bit weights are subtracted by switching the bottom plates of the capacitors from the reference voltage (V_{REF}) to ground, starting with the MSB. When switching the capacitor 32C to ground by setting bit 6 to “0”, a step of V_{REF}/2 is subtracted from the array top plate. If the input signal value is below V_{REF}/2 the comparator produces a logic “0” at the output, fixing the bit 6 at “0”. Otherwise, if the input signal value is above V_{REF}/2 the comparator produces a logic “1” at the output, returning the bit 6 to “1”. The process continues with capacitor 16C (that subtracts a step of V_{REF}/4 from the array top plate) to determine bit 5, and so on, until bit 1 is reached and the conversion is complete.

![Figure 3: Simplified schematic of a 6-bit SAR ADC](image)

**Evolving the SAR architecture for high speed and low power**

The traditional topology described above is simple; however, it is inherently slow and makes use of large capacitor arrays for moderate and high resolutions, which impact both area and power dissipation. On the other hand, this topology can be improved with a multitude of techniques that fully exploit the architecture potential for low power and increase the conversion speed.

**Reducing clock speed requirements**

The need of a high frequency clock is removed by controlling SAR and DAC blocks (Figure 2) with an internal clock that is asserted every time the comparator completes a decision. This is possible since the comparator can produce a logic signal when it completes a comparison: typically, before comparison its two differential outputs are both reset at VDD (or ground depending on the implementation), and after the comparison they become complementary. Therefore, a NAND gate produces a logic “1” when one of the outputs reaches “0,” indicating a decision was reached (an OR gate is used for reset to ground). This signal, together with a delay block, can then be used to sequence the bit decisions in succession until the conversion is complete. This way, the SAR ADC only requires a clock signal having a frequency equal to the intended sampling rate.

**Reducing capacitor array**

The capacitor array is binary-weighted, which means its size increases exponentially with the ADC resolution, doubling for every additional bit. For a 12-bit ADC, the capacitor array will grow 4096X over the minimum capacitance. A large capacitance leads not only to large area but also to large consumption on charging and discharging the capacitors during the conversion process. The solution to reduce the capacitance is to break the array in two by having a floating secondary array processing the lower order bits. For example, the same 12-bit ADC would have two 6-bit arrays, one to process the 6 higher order bits and another one interconnected to the first by a small scaling capacitor, C_{bridge}, to process the 6 lower order bits, requiring in total capacitance of only 128X the minimum capacitance.
In any case, the total capacitance of the array cannot be too small because of matching and thermal noise requirements. The matching is a function of total capacitance and, roughly speaking, errors below $C/2$ must be achieved on each capacitor to avoid missing codes. This will determine a minimum size for the unit capacitor $C$. Thermal noise also sets a minimum size for the capacitor array through $kT/C$, but normally the comparator noise dominates when the capacitor size already satisfies the matching requirements.

**Calibrating the capacitor array**

Calibration may be employed to measure capacitor matching errors, thus reducing the total capacitance to the value dictated by the noise constraint. The measurement of the matching errors can be done by observing that the nominal value of each capacitor is equal to the sum of the remaining lower order capacitors in the array. This comes naturally from the binary weighted nature of the capacitor array with an additional unit capacitor included: $32C=16C+8C+4C+2C+C+C$. The process is the following: first, capacitor $32C$ is charged to $V_{REF}$ and the remaining to ground with the top plate connected to ground. Then the top plate is opened and the connections of the capacitors are interchanged. If $32C$ has the ideal nominal value, the voltage at the top plate remains at zero. But if there is an error, the top plate voltage will deviate showing the error and making it possible to apply a calibration method. The higher density available in advanced technologies favors the use of digital calibration techniques.

**Using the capacitor array effectively**

Top-plate sampling as shown in Figure 3 causes non-linearity due to the charge-injection when the sampling switch is opened. Therefore, bottom-plate sampling is typically used: it requires additional switches on the bottom-plate of the capacitors that connect to the input signal during sampling, while the top-plate switch connects to ground. Charge injection in the top-plate can now be made signal independent, thus just causing an offset which is easily corrected with calibration.

The capacitor array may consume a significant amount of power with the charging and discharging of the capacitors between $V_{REF}$ and ground. For example, Figure 3 shows that to determine each bit, the respective capacitor is switched to ground, but later, according to the comparator decision, it may be necessary to connect it back to $V_{REF}$ — this is a source of inefficiency. Alternative switching schemes can be used to save charging energy. For example, after sampling, the bottom plates can be set to $V_{REF}/2$ instead of $V_{REF}$, and the MSB decision can then be taken immediately. This allows saving one capacitor on the array (the $32C$ in Figure 3), and prevents capacitors from switching back and forth between $V_{REF}$ and ground during the conversion.

**Improving settling time**

The main limitation to speed is the time required for the accurate settling of the capacitor array in each of the bit decisions. The voltage on the top-plate needs to settle to within half the LSB weight to avoid decision errors. That is 0.01% for 12-bit conversion, requiring over nine time constants. However, in a N-bit ADC, only once during the N bit decisions is the input voltage to the comparator so small. And only the initial bit decisions need a longer time for settling because the voltage steps are progressively smaller along the conversion. Therefore, by including redundancy in the conversion algorithm, it is possible to correct for initial errors, thus allowing the bit decisions to run faster. Redundancy can be designed in by duplicating a capacitor in the middle of the array and using it to re-center the decision range even if a previous error causes the conversion to diverge.

**Parallelizing for high speed**

Further speed improvement is possible by time-interleaving multiple SAR ADCs. This is a common technique also used with other ADC architectures, and allows achieving high sampling rate by using several lower speed converters. Interleaving four ADCs improves speed by 4X. Naturally, any offset, gain and sampling time mismatches between the interleaved ADCs will cause pattern noise and spurs in the digitized output signal and need to be corrected by calibration.


**Synopsys 28-nm SAR ADC IP**

Synopsys’ new generation of high-speed ADCs for 28-nm processes has migrated from the pipeline architecture to the SAR architecture, and was specifically engineered to take advantage of the high-speed of the process to minimize area and power consumption. Moreover, this architecture is likely to reap benefits similar to those observed in digital circuits when applied to even smaller process nodes: higher operating speeds with lower power and area.

The baseline ADC resolution is 12-bit at a conversion rate of 80 MSPS. By implementing the techniques described above, an impressive 3x lower power dissipation was achieved compared to the previous generation Synopsys ADC, which had similar specifications and was based on the pipeline architecture. The SAR architecture offers a very compact structure with only a capacitor array, a comparator and a logic block, resulting in an area reduction of up to 6x (see Figure 4).

![Figure 4: Layout comparison of a 12-bit pipeline ADC (left) to a 12-bit SAR ADC (right) with similar performance requirements for an LTE application (single channel example)](image)

By interleaving two or four data converters, the conversion rate achieves 160 MSPS or 320 MSPS (Figure 5). Each configuration is deployed as a single channel and a dual, matched IQ, channel ADC, typically used for wireless communications interfaces. This ADC parallelization can be further extended to achieve sampling rates beyond 1 GSPS.

![Figure 5: Modular design of SAR ADC](image)

Achieving these large power and area reductions require a number of design techniques, some of which are made possible by the speed of the 28-nm processes:

- Internal building blocks are dynamic, resulting in a perfect scaling of power consumption with sampling frequency.
- The capacitor array is digitally calibrated to allow sizing by the noise constraint only, and not matching. The calibration is run at start-up and does not need to be updated after supply or temperature variations because only stable and drift-free capacitor ratios need to be corrected. In the interleaved construction, the calibration corrects also for offset and gain mismatches.
Operation is asynchronous, requiring only a clock rising edge to start the conversion. The internal processing of the sampled signal and the bit decisions are sequenced by the comparator ready signal and timing circuits.

The operation is mostly insensitive to the clock duty cycle, and the ADC latency is only 2 clock cycles.

To facilitate the integration of ADCs into SoCs, the top-level interfacing is maintained as in previous generation pipeline converters. Additionally, calibration constants, which are determined after the first power-up, can be stored and reused on subsequent power-down cycles, thus reducing the power-up time in normal operation. This characteristic, together with short latency and the absence of requirements for a high-frequency clock, make this SAR-based ADC architecture especially suitable for low duty-cycle applications or other applications where the time to availability of the sample may be critical.

**Synopsys 28-nm DesignWare High-Speed Data Converter IP**

Synopsys DesignWare® Analog IP includes the SAR-based High-Speed Data Converter IP in 28-nm processes. In addition, the IP portfolio includes 12-bit 320 MSPS, 160 MSPS and 80 MSPS Receive ADCs, 12-bit 600 MSPS Transmit DACs, 3 GHz Low Jitter Clock Generating PLLs, and 12-bit General Purpose 5 MSPS ADCs and 20 MSPS DACs. Additionally, Synopsys’ analog interface portfolio includes 10-bit 300 MSPS Video DACs and 96-dB Analog Audio Codecs.

Together, these IP products make up a complete portfolio of advanced analog IP solutions that enable SoC designers to take advantage of the benefits of process scaling in terms of area and power consumption, while integrating a complete analog interface for applications such as mobile communications (LTE and LTE-A) and wireless connectivity (WiFi 802.11ac), digital TV and satellite reception, mobile applications such as tablets and smartphones, as well as other multimedia analog interfaces in the digital home.

**Summary**

In this paper we compared the main ADC architectures and concluded that the SAR ADC is now very well positioned for implementation of ADCs in modern SoCs, especially in 28-nm and beyond, because it optimally exploits the high speed and high processing power offered by these technologies.

The new generation of Synopsys ADCs available in 28-nm applies specific techniques to improve the traditional SAR architecture and achieves 3X lower power consumption and 6X lower area compared with previous generation ADC with similar specifications based on the pipeline architecture.

With more than 15 years of experience in developing analog IP solutions, Synopsys offers a comprehensive portfolio of more than 100 silicon-proven DesignWare® Data Converter IP products consisting of ADCs and DACs, auxiliary converters and analog front-ends (AFEs). Synopsys’ strong application expertise in areas such as broadband wireless communications (i.e., LTE/LTE-A, WiFi 802.11n, WiFi 802.11ac), wireline communications (i.e., G.hn, MoCA), IF demodulation, video, imaging and multimedia enables us to deliver high-quality data converter IP that help customers meet the specific design requirements for their target applications. The DesignWare Data Converter IP products offer very high performance, high speed, ultra low power dissipation, small area and support a wide range of foundry process technologies ranging from 180-nm to 28-nm.

For more information, visit: [http://www.synopsys.com/IP/AnalogIP/DataConversion/](http://www.synopsys.com/IP/AnalogIP/DataConversion/)

**References**