Dual, low-noise JFET has low capacitance and high input impedance

Steve Taranovich - August 08, 2013

Linear Integrated Systems announced the LSK489, an N-channel monolithic dual JFET with 1.8 nV per square root Hz noise at 1kHz and low-capacitance (Ciss = 4pF). This lower capacitance will greatly improve intermodulation distortion with increasing frequency with the help of the JFET’s 1 TΩ input impedance. The combination of the 1 TΩ and 4 pF input says that as frequency increases, the device will maintain its high input impedance better than most JFETs.

This JFET is part of a family of ultra-low-noise, dual JFETs specifically designed to provide users better-performing, wider bandwidths and cheaper solutions for obtaining tighter IDSS (drain-source saturation current) matching and better thermal tracking than matching individual JFETs. The company also has an in-house fab which is an indication that it can maintain good process control over production lots by tweaking the process as needed in real time as well as monitoring production to increase it for high volume demand customer needs.
Available in surface mount packages and ROHS compliant versions, the device is an ideal improved functional replacement for existing JFETs that have similar noise characteristics but greater gate-to-drain capacitance.

The most significant aspect of the device is how it combines a noise level nearly as low as the LSK389 while having much lower gate-to-drain capacitance, 4pF versus the 25pF. While the LSK389 provides ultra-low noise of less than a 1nV at 1kHz, the capacitance is high enough to cause designers to have to use a cascode feature to handle higher bandwidths without intermodulation distortion.

I include the following commentary by John H. Hall, which is not something I normally do in a product review. The reason I value what Hall has to say is his background:

• John Hall has nearly 40 years of semiconductor design work and over 60 fundamental patents, including pioneering work in low-power CMOS integrated circuit technology.

• He co-founded Intersil with Fairchild Eight member Dr. Jean Hoerni and led all technical development there.

• He has developed advanced electronics for medical, military, telecommunications and other industries.

• John Hall has provided decisive technological advantages to cutting-edge devices

- CMOS technology and electronic watch application (Seiko);
- First computerized heart pacemaker (Medtronic)
- First electronic camera shutter (Canon)
- First printing calculator (Seiko)
- First pocket pagers (Harris, Kokusai)
- Cellular phone technology (Nokia)
- First Radiation-Hardened Computer
- First Dielectric Isolation IC
- Developed Low Cost Chip Assembly for B-1B Bomber Phased Array Radar Control Module Assembly for Westinghouse Defense Systems
- Developed Highest Performance Amplifier and A/D IC Subsystem for Strategic Defense Initiative Infrared Focal Plane Sensor Array for Aerojet General

John H. Hall, President and CEO commented, “The slightly higher noise of the LSK489, versus the LSK389 (0.8 nano volts), is not significant in most instances, while the much lower capacitance enables designers to produce simpler, more elegant circuit designs with fewer devices that cost less in production.” Hall went on to say, “Though the cascode is an effective technique for compensating for some undesirable transistor characteristics, the downside of using it is in higher circuit noise. In a cascode configuration, the noise of each transistor is combined. The LSK489’s lower capacitance obviates the need for a cascode configuration in most circuit designs.”

The LSK489 features a unique Monolithic Dual design construction of interleaving both JFETs on the same piece of silicon to provide excellent matching and thermal tracking and a low-noise profile having nearly zero popcorn noise.

Summary of Features:

• Low noise (typically 1.8 nv/sqrtHz @ 1kHz)
• Nearly zero popcorn noise
• IDSS (drain-source saturation current) matching to 10% max
• Low offset/tight matching (|Vgs1- Vgs2| = 20mV max)
• Low capacitance (CISS=4 pf)
• High input impedance
• High breakdown voltage (BVGSS = 40V Min)
• Monolithic Dual (2 JFETS on one piece of silicon, better matching and thermal tracking)
• Low noise, reduced device count alternative for the classic dual JFET cascode configuration
• Improved replacement for Siliconix U401 series
• Surface mount SOIC versions and the smaller SOT23-6 package
• Lead-free ROHS compliant versions available

**Applications:**
Microphone amplifiers; phono preamplifiers; audio amplifiers and preamps; discrete low-noise operational amplifiers; battery-operated audio preamps; audio mixer consoles; acoustic sensors; sonic imaging; and instrumentation amplifiers; wideband differential amplifiers; high speed comparators; impedance converters

**Price:** US$6.37 each (1,000 pcs TO-71)

**Packages:** SOIC-8, TO-71 and SOT23-6 package options

[LSK489 dual JFET datasheet](#)

For more information visit Linear Integrated Systems [website](#)

**Also see:**
[Product How-to: LSK489 Application Note](#)
[Your friend, the JFET.](#)
[Op amps make JFET circuits repeatable](#)
[Simple circuit lets you characterize JFETs](#)

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