Book: Constraining Designs for Synthesis and Timing Analysis

Brian Bailey - August 12, 2013

The book Constraining Designs for Synthesis and Timing Analysis: A practical guide to Synopsys Design Constraints (SDC) written by Sridhar Gangadharan of Atrenta and Sanjay Churiwala of Xilinx is a highly readable book that enabled me to understand the complexities of a design task that I have never had to perform myself. In that regard, this review must be taken as coming from someone who is a novice and who did not have the opportunity to find out if I had learned the subject enough to be able to practice it myself. I also want to point out that while one of the authors of this book comes from an EDA vendor it is completely unbiased and at no place does it even mention tools that Atrenta may have available to help with the problem – so rest assured that this is not a thinly disguised sales pitch.

Contents and Excerpt

1. Introduction
2. Synthesis Basics
3. Timing Analysis and Constraints
4. SDC Extensions through TCL
5. Clocks
6. **Generated Clocks** - This chapter is excerpted [here](#). I was asked by Springer not to publish the entire chapter, so it has been cropped. The missing segments are – Shifting the edges, More than one clock on the same source, enabling combinational path and generated clock gotchas.

7. **Clock Groups** - This chapter will be excerpted in the future

8. Other Clock Characteristics

9. Port Delays

10. Completing Port Constraints

11. False Paths

12. Multi-Cycle Paths

13. Combinational Paths

14. Modal Analysis

15. Managing your Constraints

16. Miscellaneous SDC Commands

17. XDC: Xilinx Extensions to SDC

**Review**

The book is well structured and reads easily. Each chapter takes on a subject and develops it well. If I have one complaint about this book it is that there is a chapter missing. They talk at several points in the book about how certain constraints are estimated, or that information is not available until a certain point in the flow. They also talk about how static timing can be useful at certain points in the flow for ascertaining different types of timing checks. While I understand that every company uses different tools and flows, I would have liked to see a chapter that talked about the writing and evolution of the constraints during the design process. What things should companies focus on at certain points in the flow? When should the constraints be updated? When should static timing be run? What useful information will it provide? This could have also included a larger, more typical example, and while I understand that the constraints files can become very large, it would have been helpful to look at something a designer may face. The actual constraints files could have been made available online and small parts of it described in the chapter.

These comments should not detract from the fact that I would highly recommend this book to anyone who needs to get acquainted with timing constraints. I feel that I could start writing them myself after reading this book.

**More information**

The book is 253 pages and lists at $119. More information can be found on the [Springer site](#) and the book is available slightly cheaper on [Amazon](#).

Has anyone read this book who has written timing constraints, or who managed to write any after reading this book? I would love to hear your views about the book.

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**Brian Bailey** - keeping you covered

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