The Robustness of Various Test Compression Techniques

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Abstract
Larger designs and the growing population of non-stuck defects have led many companies to adopt test compression techniques. In fact, the Embedded Deterministic Test (EDT) technology within Tessent™ TestKompress® has now been used in over one billion production chips. There has been a surge of compression techniques promoted in the industry since Tessent TestKompress was released in 2001. So, why has Tessent TestKompress become the standard approach in industry? This paper will explain the technology behind the various compression techniques and their robustness in the presence of Xs, false and multicycle paths, low pin access, and other design factors.
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Executive Summary

Scan compression has become a necessity for meeting test costs and quality requirements of today’s nanometer designs. When considering a scan compression technology, several key factors should be considered in order to ensure that the compression technology does not take anything away from the existing high quality, low cost test. Some of the key areas are:

- Impact on test quality (test coverage)
- Data and time compression (tolerance to X sources)
- Low pin count testing (to enable multi-site testing)
- Design intrusion
- Area and layout overhead
- Diagnostics and impact on manufacturing flow

This paper examines several proposed and commercial compression solutions and determines the advantages and limitations of each technology in these areas. An effective compression technology must maintain the same high quality of test that can be obtained with uncompressed patterns. Low test quality in terms of coverage and fault models considered, has a direct impact on test escapes (DPM) and the ability to address yield issues. Additionally, achieving high compression of test data and time should not be intrusive to the design nor result in large area and routing overhead. Finally, in order to ensure successful and rapid defect analysis for parts that fail test on the tester, fast and accurate diagnosis of compressed test patterns is essential.

Although all methodologies address some of these key issues, only TestKompress’ Embedded Deterministic Test (EDT) technology is able to simultaneously address the requirements of high data and time compression, ability to handle X states, and suitability of compressed patterns for diagnostics while maintaining the same high quality test as uncompressed ATPG. Tessent TestKompress can achieve more than 100x compression in test data volume and testing time, in addition to maintaining high test coverage around 99%.

<table>
<thead>
<tr>
<th></th>
<th>Tessent TestKompress (EDT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decompressor</td>
<td></td>
</tr>
<tr>
<td>Encoding capacity</td>
<td>Very High</td>
</tr>
<tr>
<td>Coverage loss</td>
<td>Very Low</td>
</tr>
<tr>
<td>Compactor coverage</td>
<td></td>
</tr>
<tr>
<td>X Masking</td>
<td>None</td>
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<tr>
<td>Aliasing</td>
<td>None</td>
</tr>
<tr>
<td>Compressed Pattern</td>
<td>Yes</td>
</tr>
<tr>
<td>Diagnosis</td>
<td></td>
</tr>
<tr>
<td>Minimum channels for 10x compression</td>
<td>1</td>
</tr>
<tr>
<td>Test Time Reduction</td>
<td>100x</td>
</tr>
<tr>
<td>Data Volume Compression</td>
<td>100x</td>
</tr>
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</table>

Tessent TestKompress can deliver the same high quality test patterns through a single scan channel, making it more suitable for modular and hierarchical DFT methodologies in large designs that are pin limited for test. For more details and a summary of each technology’s performance, see the table at the end of this paper.
Introduction

Why Compression

Originally, companies realized a need for compression because of rising tester costs. The test pattern data volume exceeded the tester memory, requiring pattern reloads and excessive test application time. Over time, that need has been supplemented with the necessity to improve test quality. New fault models and additional test patterns are needed to detect new types of defects and meet the quality levels of nanometer designs. The undesirable option of pattern truncation results in lower test coverage and ultimately an increase in defective parts per million (DPM) that are shipped to customers. Therefore, in order to avoid an increase in test escapes due to low test quality, the industry has recognized an inevitable need for test pattern compression.

Goals of Scan Compression

Given that the goals of scan pattern compression are to lower tester costs and maintain high test quality, we need to identify the specific requirements for an effective compression technique.

Test Cost

- Reduce the requirement of scan data memory
- Reduce test application time per part
- Reduce the number of required scan channels
- Reduce simulation time for serial load patterns

Test Quality

- Ability to support and compress all pattern types to fit within tester memory
- Ability to support and compress patterns for several different fault models
- Ability to maintain high at-speed test coverage in the presence of many X sources
- Diagnostics of compressed scan patterns

The key requirement of any compression technology is preservation of high test quality when compared to standard (uncompressed) ATPG. In practical terms, this means that the same faults should be detected regardless of the ATPG technique used. Fault detection is achieved by specifying certain bits within the scan chains to deterministic values and fault simulating the pattern in order to determine the detection level achieved. In standard ATPG, every scan cell can be specified to the desired value simply by shifting in the scan cell value. In scan data compression technology, fewer bits are loaded so the compression hardware must be able to deliver the desired values to the appropriate scan cell in order to facilitate detection. Therefore, higher compression can be achieved by compression technologies that have greater encoding capacities, meaning that they are capable of specifying a larger percentage of the scan cells. We will utilize the concept of “encoding capacity” in this discussion and examine the design characteristics which may reduce a compression technology’s ability to specify bits and consequently compress scan data and test application time.
Compression Technologies

Several technologies have been developed over the years in order to meet the compression goals outlined in the previous section. We will briefly explore some of the better-known methodologies and highlight their advantages and disadvantages in the following section.

Virtual Scan

The Virtual scan architecture consists of an Illinois scan type decompressor on the scan chain inputs and an XOR tree based compactor on the scan chain outputs. Named after its birthplace at the University of Illinois [3], the Illinois scan decompressor reduces test data volume by broadcasting the same input data to several scan chains. Figure 1 shows 4 scan chains driven by the same scan-in pin. If any of these 4 chains require a logic value different from the logic values on the other 3 chains at the same scan-in cycle, then such a pattern cannot be applied on the tester. This restriction may result in patterns requiring such faults to be left undetected, resulting in a need for top-up ATPG using the uncompressed bypass mode. Whenever there is any such constraint on pattern generation, it will also result in more patterns for the same fault list. The biggest advantage of Illinois scan decompressor is its simplicity and low area overhead.

The scan chain outputs are compacted using an XOR tree as shown in Figure 1 below.

![Figure 1: Virtual Scan Configuration](image)

Fault effects captured on any of the four scan chains connected to an output channel can be observed through the XOR tree compactor, as long as the there are no Xs captured on the same scan_out cycle. Presence of Xs will result in loss of fault coverage, or result in generating more test patterns. If a fault effect is captured in more than one scan cell, and an even number of those fault effects appear on the inputs of an XOR tree in the same scan_out cycle, none of them will be observed on the scan_out channel. This is called fault aliasing, and results in loss of coverage, or increase in number of patterns.

Table 1 below shows results of regular ATPG with Tessent™ FastScan™ and the two compression techniques using Tessent TestKompress and Illinois Scan decompressor. The scan chain outputs were observed directly (without using any XOR tree compactor) in these
experiments. In all cases, Illinois scan shows higher data volume compared to Tessent TestKompress.

Table 1: Experimental results using Tessent FastScan, Tessent TestKompress and Illinois scan

<table>
<thead>
<tr>
<th>Design</th>
<th>Test Method</th>
<th>Channel/Chain Ratio</th>
<th>Test Coverage</th>
<th>Normalized Test Coverage</th>
<th>Normalized Pattern Count</th>
<th>Normalized Scan Volume</th>
<th>Normalized Compression Ratio</th>
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</thead>
<tbody>
<tr>
<td>A</td>
<td>Tessent FastScan</td>
<td>1600/1600</td>
<td>97.06%</td>
<td>96.75%</td>
<td>8215</td>
<td>578M</td>
<td>1.0</td>
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<td>96.75%</td>
<td>9965</td>
<td>7.7M</td>
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<td></td>
<td>Illinois Scan</td>
<td>16/1600</td>
<td>96.75%</td>
<td>96.75%</td>
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<td>10M</td>
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<td>0.8M</td>
<td>32.1</td>
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<td>95.16%</td>
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<tr>
<td></td>
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<td>98.17%</td>
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<td>2.8M</td>
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<td>D</td>
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<tr>
<td></td>
<td>Illinois Scan</td>
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<td>96.95%</td>
<td>96.95%</td>
<td>12799</td>
<td>11.7M</td>
<td>16.5</td>
</tr>
</tbody>
</table>

Advantages of Virtual Scan

- Very simple architecture. No extra logic gates used on scan chain inputs.
- Good compression, very close to the ratio of scan chains to scan channels.

Limitations of Virtual Scan

- High fan-out nets between scan channels and internal scan chains may result in high routing congestion.
- Linear dependencies between scan cells on the same scan cycle will result in loss of controllability, leading to loss of coverage in compression mode.
- Top-up patterns in bypass mode may be required to improve test coverage.
- Loss of coverage in the XOR tree compactor due to X values captured in scan cells and fault aliasing effects.
**Adaptive Scan**

The adaptive scan technology uses a modified Illinois scan structure at the inputs and a modified XOR tree structure at the outputs. The decompressor is very similar to Illinois scan, but uses multiplexers ahead of the scan chains [4,5]. The select data for the multiplexers are also loaded from the tester allowing some flexibility in the data loaded onto the scan chains from a single scan channel. Figure 2 below shows one implementation of adaptive Illinois scan.

![Figure 2: Adaptive scan architecture](image)

In the figure shown above, Channel 1 drives the select lines of the multiplexers, and is loaded from the tester with different values in each cycle. The second and third scan chains can be loaded with different values in each cycle by a proper selection of values loaded into Channel 1. A general structure of adaptive scan will consist of one or more levels of muxes in front of every scan chain, and one or more channels to drive the select lines of those muxes. In order to improve coverage and compression, adaptive scan configurations require at least one scan input to drive the mux-select lines and at least two other scan channel inputs.

A simpler approach is to change the mux-select line on a per pattern basis (rather than per cycle) in order to allow for faster scan chain loading. In this technique, the mux-select line only changes between pattern loads and remains static during scan shifting. This alternate scheme increases the restrictions on the ATPG tool and will result in increased pattern count.

The XOR tree compactor on the scan chain outputs is modified [5] to observe certain scan chains on more than one scan channel. This kind of fan-outs will enable fault effects to be observed on a second scan channel if it gets masked on the first channel due to Xs, or due to fault aliasing effects. The side effect of this fan-out structure is that, an X on a scan chain that fans out to more than one channel will end up masking a lot more fault effects than a simple XOR tree.

Figure 3 below shows the rapid drop in test coverage when using XOR tree based compactors like the one used in Adaptive Illinois scan architectures. This example used 1600 scan chains compacted onto 13 scan channels. The effects of the coverage drop can only be minimized by...
increasing the number of scan channels, resulting in a reduction of compression that can be achieved.

![Graph](image_url)

**Figure 3: Effect of X values on test coverage**

### Advantages of Adaptive Illinois Scan

- Better encoding capacity and reduced linear dependencies on scan cells than regular Illinois scan.
- Better observability of fault effects through the modified XOR tree compactor.

### Limitations of Adaptive Illinois Scan

- Multiplexers and high fan-out nets on scan chain inputs resulting in some area overhead and routing congestion.
- Some linear dependencies on scan cells may require top-up ATPG patterns to be generated in the bypass mode.
- Commercial approaches require a minimum of 5 scan channels to reach as little as 10X compression.
- Changing mux-select with each shift cycle can result in timing issues during shift.
- The XOR tree compactor still does not guarantee detection of all fault effects in the presence of Xs and fault aliasing effects.
On-Product Multiple Input Signature Register (OP-MISR):  
The OP-MISR architecture [1,2] is adopted from the logic BIST principles, but used for testing devices on a tester (ATE). The architecture of OP-MISR is shown in the Figure 4 below:

![OP-MISR architecture](image)

The key idea of this architecture is to use on-product signature generation to eliminate the bandwidth and any data volume overhead for external response collection in the ATE while continuing to supply ATPG test stimuli from the ATE. In the figure 4, Si/So is a bidirectional scan pin whose directionality is controlled by “sdir”. The control signal “mrun” enables or disables the MISR feedback connections. For mrun=1 the MISR is configured as a signature register and compresses the scan chain outputs. When mrun=0 the MISR bits are connected in series with the scan chains, such that the scan chains and the MISR contents can be unloaded to the tester through the bidirectional scan pins. The Mask logic along with “mske” from tester will provide the X logic masking capabilities, required to avoid corrupting the MISR signature.

The output response compaction with MISR can result in about 10-20x compression in data volume. The use of bidirectional pins for scan chains can double the number of scan chains used in a traditional arrangement. The resulting scan chains will be half in length, resulting in a test time reduction of 2x [1,2].

OP-MISR+ [2] uses an Illinois scan type of configuration on the input side resulting in better compression in terms of testing time. OP-MISR+ improves the test time reduction from 2 to 11.

Advantages of OP-MISR
- Deterministic ATPG patterns delivered directly from the tester.
- No test points required, and no loss in coverage due to encoding capacities or linear dependencies.
- Good compression of data volumes.

**Limitations of OP-MISR**
- Test time reduction limited to 2x in OP-MISR, and about 11x in OP-MISR+.
- Failure diagnosis requires retesting with MISR bypassed.

**Embedded Deterministic Test (EDT)**
EDT [6] was developed primarily to reduce the testing time and test data volume on large multimillion gate designs that need testing for several fault models. Tessent TestKompress is the tool that can generate the decompressor and compactor logic at the RTL level. The architecture consists of a decompressor and a compactor embedded on the chip. The decompressor drives the scan chain inputs and the compactor connects from the scan chain outputs. The Tessent TestKompress logic is inserted only in the scan path as shown in Figure 5. In the presence of Tessent TestKompress logic we can have a large number of very short scan chains.

![Figure 5: EDT architecture](image)

Test patterns are generated by targeting individual faults in the core, and are converted to compressed stimuli and compacted responses to be applied through the Tessent TestKompress logic. The pattern generation algorithm and the fault models used are totally independent of the Tessent TestKompress logic. Since the patterns are generated deterministically, we can obtain very high coverage of the modeled faults with a very compact set of test patterns. There is also no need to add any test logic in the core to improve testability, as the patterns are generated deterministically.

The decompressor consists of a ring generator (unlike a Type I or Type II LFSR) as shown in Figure 6.
The outputs of the ring generator flops will connect to scan chain inputs through a phase shifter consisting of XOR gates. Creation of the compressed stimuli from a test pattern consists of solving a set of linear equations based on the ring generator polynomial and the phase shifter connections. Inputs to the ring generator are driven from the compressed stimuli on the ATE. The output response compactor consists of an XOR tree and the masking logic, as shown in Figure 7.

The masking logic consists of a pattern mask register, decoder, and AND gates before the XOR tree. The logic values for the pattern mask register are loaded from the compressed pattern data on the ATE. The masking logic and the XOR tree compactor have the ability to handle any number of unknowns (Xs) from the scan chains without any modifications to the functional logic. The masking logic will also eliminate the effects of fault aliasing through the XOR tree. The decompressor/compactor logic implemented in TestKompress can also perform fault diagnosis using the same compressed patterns that is used on the ATE.

The Tessent TestKompress logic architecture is highly scalable. The ratio of internal scan chains to external scan channels gives an indication of the possible reduction in testing time and test data volume, compared to conventional scan testing with deterministic test patterns. There are other factors that also determine the actual amount of compression that any design can obtain.

Advantages of EDT
- Best encoding capacity.
- Linear dependencies are completely eliminated by the phase shifters.
• A single scan channel can be used to obtain time and data compressions of more than 100x.

• No routing congestion, as there are no high fan-out nets. Modular implementation can be used for easy block-level implementation.

• All faults that propagate to scan cells are guaranteed to be detected by the automated masking capability of the compactor, even in the presence of any number of Xs and fault aliasing.

• No need to generate any top-up ATPG patterns as the test coverage in the compressed and bypass mode are the same.

• Compressed patterns can be directly diagnosed for failures found on the tester, and there is no loss of diagnostic resolution compared with bypass mode patterns.

Limitations of EDT
• The ring generator, phase shifter, XOR tree compactor and the x-masking logic contributes to an area overhead of up to 1% generally.

Design Characteristics and their Impact on Compression
Compression Limits
Is compression ever “good enough”? The limits on test data and test time reduction can be estimated from the ratio of scan chains to scan channels. The test data reduction also depends on whether one is using compactor logic, or MISR based compression logic. The actual value of test data and time reduction depends on various factors, some of which are:

• Encoding capacity of the Decompressor logic
• Handling of unknown logic (X) values and fault aliasing by the compactor logic
• Number of X sources that propagate to scan cells in the design

X Sources
Unlike standard ATPG, any logic that produces unknown (X) states can result in difficulties for compression technologies. All MISR-based methodologies, such as OP-MISR, require additional masking logic in order to prevent any unknown states to be captured into the scan chains and ultimately the MISR. Sources of Xs include un-initialized and uncontrollable flip-flops, bus contention, floating buses, multiple clock domains, false and multicycle paths, and inaccurate or incomplete simulation models.

Compactors without X masking are greatly impacted by X sources and will have lower coverage because they must use bypass (uncompressed) patterns to achieve high test coverage. Compression may be “good enough” for stuck-at faults but for transition faults, the introduction of false and multicycle paths introduces many more X sources to the design. Compression will greatly suffer as a result of the additional X sources. The following table 2 shows the actual compression obtained by TestKompress logic, in row labeled Comp. for several industry designs of various types and sizes. The table also shows the maximum number of specified bits and the number of unknown value sources (#Xs) within the design. The the row labeled Channels:Chains indicates the number of channels and chains used in that design.
Table 2: Experimental results with Tessent TestKompress logic

**Design Flow Flexibility**

Tessent TestKompress, incorporating the EDT technology, provides very flexible flow options. Given a scan inserted netlist, the RTL Tessent TestKompress logic can be created by specifying the number of external channels. The logic can also be created early in the design flow by simply defining the number of scan chains and the clocking for the first and last scan cells in every chain. The logic is pattern independent and need not be recreated following ECOs as long as the number of chains and channels are not changed. During the RTL logic creation phase it is also possible to perform compressed pattern generation if the synthesized design core is available at the gate level.

Tessent TestKompress logic can also be inserted at the block level, independent of other blocks in the design, and not requiring any top level logic. The flow can be simplified as the tool can have as few as one scan channel for each block. Modular Tessent TestKompress allows us to run ATPG in parallel for all the blocks that have the logic as well as any uncompressed scan chains, without requiring wrapper chains around blocks. In addition, it can be implemented in a hierarchical manner where each block is tested individually using top level muxing logic. Modular Tessent TestKompress has been successfully used in large industrial designs with a volume production of 10 million chips [12].

**Area Overhead and Layout Constraints**

Another concern for designs with compression technology is the additional area overhead required. If area overhead exceeds established limits, it may be required to move to the next larger die size but that can be quite costly. It is important to note that area is effected by two aspects, gate count, and routing area.

With regards to compression, difficulties can be encountered because many scan chains must be connected to the decompression and compression logic resulting in huge fan-out nets.

The decompressor/compactor logic generated by Tessent TestKompress requires a small number of simple gates for every scan chain in the design. The routing overhead is very minimal as there is no huge fan-out within Tessent TestKompress logic or with its connections to scan chains. The routing overheads (if any) can be minimized by either segmenting the decompressor/compactor, or using Modular Tessent TestKompress.
The Virtual scan architecture does not have any logic gates on scan chain inputs, but has a huge fan-out net from every scan channel to the scan chains, resulting in a large area overhead due to routing. The adaptive Illinois scan adds a multiplexer in front of every scan chain, in addition to the huge fan-out nets and the routing overhead.

The area overheads due to the XOR tree-based compactor architectures depend on the number of XOR gates added on the scan chain outputs. The adaptive scan compactor logic also has huge fan-out nets from each scan chain output to multiple points in the XOR tree.

Manufacturing Test

**Impact of Compression on Test Quality**

All the test compression techniques discussed above rely on the fact that not all scan cells need a defined logic value to detect any fault. The defined logic values on scan cells is also referred to as a test cube for the targeted fault. As long as the number of defined scan cell values is a small percentage of the total number of scan cells, most of the decompressor logic options discussed in this paper will be able to deliver those values without much impact on test coverage and the number of test patterns. The undefined scan cells will be defined by the values that can be delivered by the decompressor logic used. The ability of the decompressor to deliver any set of values on the defined scan cells is also known as the encoding capacity of the decompressor. Decompressors with low encoding capacity will not be able to deliver certain test cubes required to detect a fault, resulting in lower test coverage, and requiring the application of test patterns in the compression bypass mode.

In addition to controllability, an effective compression methodology must be able to observe the circuit responses through the compactor logic. The ability to handle a large number of unknown states while maintaining high observability will greatly impact the compression solution’s ability to achieve high test coverage while maintaining a high compression ratio.

Of all the compression technologies discussed in this paper the Tessent TestKompress decompressor (ring generator) has the highest encoding capacity while the patented masking logic in the tool provides for guaranteed observability of fault effects. This has been demonstrated on hundreds of designs which show no loss in test coverage when generating highly compressed patterns, compared to generating patterns in bypass mode.

Diagnostics

Diagnosis is the process of identifying defects or fault locations that resulted in failures caught on the tester. The test patterns generated for different fault models are applied to the manufactured device on an Automatic Test Equipment (ATE). If the measured logic value on the device outputs does not match with the expected logic values in the test patterns, it is due to a manufacturing defect. Diagnosis tools like Tessent™ Diagnosis can identify the fault locations that resulted in those failures. Inputs to Tessent Diagnosis could be regular ATPG patterns, or compressed ATPG patterns from Tessent TestKompress.

Tessent Diagnosis analyzes (by simulation) the actual responses from the tester and determines which faults might have caused the observed failure effects. This method does not require building a huge database fault dictionary, and is very effective in diagnosing both compressed and uncompressed test patterns [7].
In an experiment on 70 manufactured devices and 10K failing patterns, it was found that 68 out of 70 devices had perfect or good matching behavior between Tessent TestKompress and regular uncompressed pattern diagnosis [8]. Several other experiments have shown that the diagnostics resolution for direct compressed pattern diagnosis is at least as good as the diagnostic resolution achieved in bypass mode with uncompressed patterns [8]. Tessent Diagnosis enabled engineers at TSMC to improve the yield by 24% for one device. The diagnosis was completed in 2 days, significantly improving the failure analysis productivity [11].

Summary
In this paper we discussed several test data and test time compression techniques. All the techniques require on-chip decompression and compaction hardware adding to area overhead in terms of logic gates or high fan-out routing nets or both. Any MISR based compression technique, like the OP-MISR, also requires additional logic to block Xs from propagating to the MISR, and bypass mode re-testing for failure diagnosis. Some of the compressors like adaptive Illinois scan require more than one scan channel to achieve any compression of test data and time. As shown in the section on adaptive scan (Figure 3), Xs captured on scan cells will result in significant loss of coverage, requiring a top-up ATPG in compression bypass mode. Unknown (Xs) will always be present in designs with false and multicycle paths, and cross clock domain logic. Any pattern generated in bypass mode will result in an overall reduction of total compression obtained.
The following Table 3 gives a quick overview of the topics discussed in the paper.

### Table 3: Comparison summary of compression techniques discussed

<table>
<thead>
<tr>
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<th>Virtual Scan</th>
<th>Adaptive Scan</th>
<th>OP MISR+</th>
<th>Tessent TestKompress (EDT)</th>
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<tr>
<td><strong>Encoding capacity</strong></td>
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<td>Low</td>
<td>Very Low</td>
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</tr>
<tr>
<td><strong>Top-up ATPG</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td><strong>Area Overhead</strong></td>
<td>Low</td>
<td>Moderate</td>
<td>Moderate</td>
<td>Moderate</td>
</tr>
<tr>
<td><strong>Compressed Pattern Diagnosis</strong></td>
<td>Possible</td>
<td>Possible</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Minimum channels for 10x compression</strong></td>
<td>&gt; 5</td>
<td>&gt; 5</td>
<td>&gt; 5</td>
<td>1</td>
</tr>
<tr>
<td><strong>Test Time Reduction</strong></td>
<td>20x</td>
<td>50x*</td>
<td>20x</td>
<td>100x</td>
</tr>
<tr>
<td><strong>Data Volume Compression</strong></td>
<td>20x</td>
<td>50x*</td>
<td>100x</td>
<td>100x</td>
</tr>
</tbody>
</table>

* results may suffer significantly when using at-speed test due to Xs introduced with false and multicycle paths, and cross clock domain logic.

As shown, the EDT based Tessent TestKompress logic can achieve very high compression of test time and data even with a single scan channel, making it more suitable for modular compression methodologies and very low pin count testing. Direct compressed pattern failure diagnosis is possible with XOR tree based compactors. TestKompress effectively works with YieldAssist to provide direct diagnostics of compressed patterns and is proven in production lines. For some more information on different compression techniques please refer to [9] and [10].

### References


