Programmable Fractional Clock Frequency Divider Circuit

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Abstract

Programmable clock frequency dividers play an integral role in contemporary SoC designs which need clocks of different frequencies in different run modes. Fractional clock frequency dividers are a special type of divider circuits where the dividing factor is a fraction. This paper presents a programmable fractional clock frequency divider which uses purely digital components and can achieve division factors in the multiples of 0.5. The paper will corroborate the results with the help of circuit diagram and the simulation results.

Keywords

Clock divider, Fractional Clock Divider, Programmable Circuit

1. Introduction

A frequency divider circuit generates an output clock signal whose frequency is a divided version of the input clock signal. The source of the input clock signal may be a PLL (Phase Locked Loop), or an oscillator external to the SoC. While most of the clock dividers divide the input clock signal frequency by an integer, it may be desirable to divide the clock frequency by a fraction. Moreover, since different run modes of the SoC may require a clock of different clock frequency, it calls for a versatile circuit which is programmable in nature. In this paper, we disclose a fractional clock divider circuit which is programmable. It must also be noted that fractional dividers cannot achieve a duty cycle of 50\% using purely digital components.

The remainder of the paper is organised as follows. Section 2 discusses the basic principle and the building blocks, eventually leading to the disclosed divider circuit. Section 3 depicts the simulation waveforms for 3 fractional configurations. Finally, the conclusions are drawn in section 4.

2. Basic Building Blocks and Rationale

This section discusses the rationale employed in the design and the basic building blocks used to accomplish the same.

2.1. Design Rationale

Dividing an input clock by a fractional division factor \(N.5\), where \(N\) is an integer means that the output clock signal would comprise of \(2N+1\) half clock cycles. It must be noted that the number \(2N+1\) would always be an odd integer. A direct consequence of the above observation is that there must be alternate transitions at positive edge and negative edge of the input clock. The disclosed circuit uses dual edge triggered flip-flops to achieve the same. Moreover, given the division factor \(N.5\), one can deterministically compute the number of half edges the output clock signal should be low and high. The below table shows the number of half clock cycles with respect to the input clock when the output clock signal is desired to remain low and high.
Table 1. Construction of output divided clock from input clock.

<table>
<thead>
<tr>
<th>Division Factor (N can be an even or an odd integer)</th>
<th>Number of half cycles when output is low</th>
<th>Number of half cycles when output is high</th>
</tr>
</thead>
<tbody>
<tr>
<td>N.5</td>
<td>N</td>
<td>N+1</td>
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</table>

2.2. Operation of the circuit

Fig.1 depicts the disclosed circuit of fractional clock frequency divider. The counter CNT shown in the figure is a dual-edge triggered synchronous binary counter with synchronous reset. As soon as the binary counter starts counting from its reset value of 4'b0000, the comparator Comp-1 keeps track of the first occurrence of binary \((N-1)\) and outputs a logic 1'b1. This triggers the synchronous reset and binary counter goes back to 4'b0000. Also, the clock gating integrated cell CGIC which is also a dual-level triggered clock gating cell, gets enabled. The de-multiplexer D now disables the Comp-1 and makes the path from counter CNT to comparator Comp-2 transparent. The comparator Comp-2 is configured to output a logic 1'b1 at the occurrence of \(N\) at the outputs of counter. This enables the CGIC for the second time and we can achieve the desired output clock signal at the output of the dual-edge triggered flip-flop FF.

![Figure 1. The proposed circuit for fractional clock frequency divider](image)

It must be noted that since comparator Comp-1 has been configured to detect \((N-1)\). For a division factor of 1.5, where \(N\) is equal to 1, the comparator Comp-1 would detect 0. Since this value corresponds to the reset value of the counter CNT, the counter in this case does not come out of reset. To achieve a division factor of 1.5, an alternate circuit is multiplexed with the above described circuit with select line of the multiplexer detecting the division configuration of...
This circuit to accomplish division by 1.5 also uses dual-edge triggered flip-flops and is depicted in Fig. 1. All the flip-flops used in Fig. 1 are dual edge triggered flip-flops. Also, the clock gating integrated cell is a dual level triggered CGIC.

2.3. Scope of the Circuit

The circuit described above can be used for division factors which are multiple of 0.5. The width of the counter decides the maximum permissible division factor the circuit can achieve. Using an n-bit counter, one can achieve division ratios from 1.5 to \(2^n/2\). For example for n = 4, the permissible division factors are 1.5, 2.5, 3.5 up to 15.5. Similarly, if one intends to attain the division factors up to 31.5, it can be done by using a 5-bit dual-edge triggered binary counter and a comparator of the same size.

3. Simulation Results

The figures 2, 3, and 4 depict the output waveforms for division factors of 6.5 and 13.5 respectively.

![Figure 2. Output waveform for division factor of 1.5](image)

![Figure 3. Output waveform for division factor of 6.5](image)

![Figure 4. Output waveform for division factor of 13.5](image)

It must be noted that except for 1.5, the duty cycle of the output waveforms invariably lies in the band of 40%-60%.
3. CONCLUSIONS

The proposed circuit uses dual-edge triggered flip-flops to accomplish division by fractional ratios which are multiple of 0.5. The circuit is programmable and the design can be extended for higher division factors by simply increasing the width of the binary counter used. The circuit is therefore versatile and uses only digital components to realize the same.

REFERENCES


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