PCB signal coupling can be a problem

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When PCB traces are in close proximity, they can talk to each other through the capacitor created by these traces. This type of cross-talk can wreak havoc as you try to combine analog and digital signals on the same board. Given this issue, there are two areas where you might want to pay attention as you strive to separate your trace signals. The first area is where two traces, on different layers, cross. The second area is where two traces run parallel on the same layer.

You can create a parasitic capacitor on your board as long as two traces are in proximity. This capacitance is equal to the permittivity ($\varepsilon_r$ and $\varepsilon_0$) of the board material times the crossover area (A) divided by the distance (d) between the two traces.

$$ C = \frac{\varepsilon_r \varepsilon_0 A}{d} \quad \text{Eq. 1} $$

The dielectric constant ($\varepsilon_r$) of FR4, a glass epoxy used for PCBs, is from 4.4 to 4.8. We will use 4.7 in our calculation. The vacuum permittivity ($\varepsilon_0$) equals $8.84 \times 10^{-12}$ F/m. **Figure 1** shows an example of two traces crossing on an FR4 PCB.

![Figure 1](image)

**Figure 1** Two 0.25 mm-wide PCB traces on two different layers with a square clock wave signal on the top layer trace.

Note: 10 mil = 0.25 mm.
The solid black lines in Figure 1 illustrate a top layer trace and the dashed red lines illustrate a second layer trace. The distance (d) between layers one and two is 0.25 mm or 10 mils. If you use Equation 1 for the Figure 1 dimensions, the capacitance between these traces is 0.01 pF.

If there is a square wave clock signal traveling down the top (black trace), the current transmitted through the parasitic capacitance into the trace on the second layer is equal to:

\[ I = C \frac{\partial V}{\partial t} \]  

Eq. 2

where \( \partial V \) equals the change in voltage and \( \partial t \) equals the change in time.

With a rise time of 10 nanoseconds for a digital signal from 0 to 5V and a capacitance of 0.01 pF, the peak current is 50 µA. You can see that this is a fair amount of current, which flows into the second trace’s impedance. If the second analog trace’s impedance is equal to 100 megaOhms, this current creates a voltage spike of 0.5 V. In the analog world, this can be a very disruptive voltage spike.

A second scenario that creates board parasitic capacitance is where two traces, on the same layer, parallel each other. Figure 2 illustrates this circumstance.

Figure 2 Two PCB traces on the same PCB layer with a square clock wave signal on one of the traces.

This capacitance is equal to the permittivity \( (e_R \text{ and } e_0) \) of the board material times the parallel length (L) times the trace thickness (w) divided by the distance (d) between the two traces.

\[ C = e_R e_0 \frac{L w}{d} \]  

Eq. 3

Again, let’s use 4.7 for the dielectric constant \( (e_R) \) of FR4 PCB and the vacuum permittivity \( (e_0) \) of 8.84 x 10\(^{-12}\) F/m.

A typical application board where this may occur is where the parallel length (L) is equal to 5 cm and the distance between the traces is 0.5 mm. If you use Equation 3 for the Figure 2 dimensions, the capacitance between these traces is approximately 0.01 pF.
These are two examples of how to build low-cost capacitors on your PCB. Unfortunately, these capacitors, combined fast-switching speeds and high-impedance analog lines to create a disaster. For instance, imagine that your switching speeds are sub-nano seconds long and your analog lines are high impedance, such as the input to an amplifier. You will see some severe signal integrity problems arise!

So what do you do? Generally, separate your digital activity from your analog activity on the board. By separation, I do not mean put these activities in separate layers. Decrease these parasitic capacitor sizes as much as possible in Figure 1 by increasing the distance between the cross-over traces. If you have a Figure 2 circumstance, decrease the length (L) of your parallel traces, increase the distance, d, between these parallel traces. Remember, d is in the numerator of the equation.

Another solution for the problem in Figure 2 is to slip a ground trace between the two traces. See Figure 3 for this solution.

![Figure 3](image)

**Figure 3** A common strategy for reducing trace cross-talk is to insert a low-impedance, ground trace between the offending traces.

Have you had these issues show up in your circuits? And more so, have you ever used these stray capacitances to your advantage? If so, please comment below on how you did that.

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*Bonnie Baker* is a senior applications engineer at Texas Instruments.

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