As the Semiconductor industry is growing so does the density of devices on chip. With the increasing density and decreasing spacing rules, the most significant effect that takes birth is parasitic. Parasitics can be of resistance or capacitance types, both have to be handled carefully. In this paper we will discuss parasitic capacitance.

In VLSI applications the parasitic capacitance between signal lines can deplete our whole design. At low frequencies parasitic capacitance can usually be ignored, but in high frequency circuits it can be a major problem. For example, in amplifier circuits with extended frequency response, parasitic capacitance between the output and the input can act as a feedback path, causing the circuit to oscillate at high frequency. These unwanted oscillations are called parasitic oscillations.

The parasitic capacitance arises from an electrical coupling between one signal line and another signal line or a signal line and the substrate. In some designs it becomes mandatory for us to reduce the parasitic capacitance of a particular net with respect to other signal. Now how it can be done? What are the different ways to be approached for that? We will discuss all these methods in this article.

**Origin of parasitic capacitance**

- Transistors
  - Depends on area of transistor gate
  - Depends on physical materials, thickness of insulator
- Diffusion to substrate
  - Side-wall capacitance-capacitance from periphery
  - bottom-wall capacitance-capacitance to substrate
- Metal to substrate
  - Parallel plate capacitance is dominant
  - Need to account for fringing, too
- Poly to substrate
  - Parallel plate plus fringing, like metal
Capacitance between conductors

- $\text{Metal}_i \ & \ \text{Metal}_i$
- $\text{Metal}_i \ & \ \text{Metal}_i+1$

At the layout level we can control parasitic capacitances which are due to the last three points among the above given points.

Following are some of the best methods we can use for decreasing parasitic capacitance:

1. Use higher metals for the net in which parasitic capacitance is important.
2. Increase the spacing of all the nets from the net which is critical (for which parasitic capacitance is important).
3. Put some other reference signal (with which parasitic capacitance is not so important) in between the nets for which lower parasitic capacitance required. This is shielding.
4. Avoid too much parallel routing of metals.

Now we will discuss all the above techniques one by one but before that let us discuss about the basic concept of capacitance.

**Definition of capacitance**

The equation for the parasitic capacitance is given by **Equation 1** given below:

$$C = \frac{eA}{d} \quad \text{Equation 1}$$

Where $e$ is the dielectric constant of an insulator disposed between the two plates of the capacitor, $d$ is the spacing between the two plates of the capacitor and $A$ is the common area of the plates.

So as the distance between the plates increases, capacitance between them decreases or as the common area between the plates decreases so does the capacitance between the two plates. In layout plates capacitance can be replaced by the signal lines. The signal width times the signal length is the area of the signal lines.

More importantly, there can be mainly two possibilities in the layout so as to see the parasitic
capacitance. This can be understood with the help of 3D view of nets. Firstly parasitic capacitance can be from sides (as shown in below diagram between M2 and M2) [case 1] and secondly it can be from top and bottom of the routing (as shown in diagram between M2 and M3) [case 2]

![Diagram showing parasitic capacitance between metal layers](image)

**Figure 1: Showing parasitic capacitance from sides of metal and from top and bottom of metal**

It should be noted that case 1 capacitance is always higher then case 2.

Now let’s discuss some important points mentioned before to take care of controlling capacitance during routing of critical nets.

**1. Use higher metals for the net for which parasitic capacitance is important.**

In this case let’s take the parasitic capacitance between higher metal and the lower metals into account i.e. parasitic capacitance between signal A and other signals (B, C, D, E, F etc.) This is similar to case 2 of Figure 1. With using higher metal we are actually increasing the distance between the plates (as in below figure signal A is with M6 and B, C, D, etc. are with M1 and in between M1 and M6 there are M2, M3, M4, M5 metals) which ultimately decreases the parasitic capacitance (as according to Equation 1)
2. Increase the spacing between the nets in which parasitic capacitance required is less.

In this case most important is the parasitic capacitance between same metals i.e. between M1 and M1 or between M2 and M2 etc. that is case 1 of Figure 1. So with increasing the space between the nets we are increasing the distance between the plates which ultimately decreases parasitic capacitance. For example in Figure 3, parasitic capacitance between one bank of signals and another bank of signals is important, so we have placed them at some distance from each other.
Another way of routing the signals can be as in Figure 4, i.e. doing routing with alternate metals, which also results in increasing the distance between the nets and ultimately parasitic capacitance. Here we have routed a signal with Metal 3 in between signals A and B which are routed with Metal 1. As a result of this distance between A and B signals have increased which resulted in decreasing parasitic capacitance between A and B.

![Figure 4: Routing with alternate metals can increase the distance between the nets and ultimately parasitic capacitance](image)

3. Put some other reference signal (with which parasitic capacitance is not so important) in between the nets for which the parasitic capacitance required is less.

![Figure 5: All routes should be with the same Metal and equidistant from each other](image)

As in Figure 5 putting the reference signal in between the nets can also serve our purpose of decreasing parasitic capacitance between the signal nets i.e. between A and B. It not only increases distance between the signal nets but the reference signal also tries to neutralize the parasitic capacitance between the signal nets. This technique is known as shielding from the sides. If your shielding has a low impedance path (e.g. good grounding), the coupled noise flows into this path, and will reduce the impact on vulnerable signals.

4. Avoid too much parallel routing of metals
Here parallel routing means one metal on another metal completely as shown in Figure 6.

**Figure 6: Signal A (Metal 2) is routed over signal B (Metal 1) in parallel, and causes a large area between the plates A and B, which in turn causes higher parasitic capacitance between the plates.**

With parallel routing there is a maximum area between the two metals so there is maximum capacitance between the two as well. So to avoid that we can do routing as in Figure 7.

**Figure 7: Parasitic capacitance is reduced with this technique as compared to Figure 6**

With the effective area overlap between the metal plates decreased, parasitic capacitance has also decreased.

Another technique is by adding some reference signal in between the two signal lines (as shown in Figure 8).
Figure 8: Signal C (Metal 2) is inserted in between Signals A (Metal 3) and B (Metal 1) so as to decrease the parasitic capacitance between A and B.

With the Figure 8 method of routing, the effective parasitic capacitance between two signal nets (A and B) decreases. Signal C acts as shielding for signals A and B. If sometimes our signal is too critical that small noise can harm it then we can do coaxial shielding also, which is covering all the four sides of the signal with a reference signal. It can be shown as in figure 9 that Metal 2 (shielded signal) is shielded from all the four sides (i.e. top with M3, bottom with M1, sides with M2).

Figure 9: Metal 2 (shielded signal) is shielded from all the four sides (i.e. top with M3, bottom with M1, sides with M2).

With the above few methods we can reduce parasitic capacitance to minimum which helps the design to perform with a great improvement in performance. It should become the practice of the Layout Designer to keep all the above steps while doing layout of any design in which parasitic capacitance is important.