Are you the 1%?

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The extent and reasons that might cause you to worry about semiconductor yield challenges depends on many factors. If your device is manufactured using a leading edge process, you probably work tirelessly and hand-in-hand with your foundry to ensure that process and product yield is ramped up more or less in parallel. If, however, your company is lagging behind a node or two, yield might not keep you awake at night, at least not until the unexpected happens.

For devices in markets such as medical and automotive, you would carefully look for anything that could indicate a quality or reliability concern. Then there are those we affectionately refer to the 1%-ers: those products that have been manufactured for a long enough time and in high enough volume that it makes financial sense to chase down that that last 1% yield loss.

With the increasing number of yield challenges, such as the dramatic increase in number and complexity of design sensitive defects, many fabless semiconductor companies are arming themselves with new technologies like DDYA (diagnosis-driven yield analysis), which can rapidly identify the root cause of yield loss and effectively separate design- and process-oriented yield loss. In a recently published case, Freescale used the results from diagnosis analysis of 1300 failing die to improve mature yield by 1.5% in a few weeks. New advances in diagnosis analysis technology make DDYA more valuable than ever before.

DDYA has two key components. First, as illustrated in Figure 1, scan diagnosis software makes failing test cycles valuable by identifying defect locations and classifications based on the design description, scan test patterns, and tester fail data.
The second component in a DDYA flow is the statistical analysis, which makes the diagnosis results from a number of failing devices actionable. The primary challenge for yield analysis based on diagnosis data is dealing with the ambiguity in the results. For example, the defective behavior seen on the tester could be explained by a defect in more than just one single location. Second, each diagnosis result, often referred to as a suspect, could have multiple possible root causes associated with it.

To effectively eliminate the noise in the diagnosis results and determine the underlying root causes represented in a population of failing devices, you can use a new technology called RCD (root cause deconvolution). This technology is based on Bayesian probability analysis, which is well-known in machine learning applications.

RCD leverages design statistics such as critical area per net segment per metal layer and count of tested cells per cell type. The technology uses a probabilistic model that calculates the probability of observing a set of diagnosis results for a given defect distribution. This model is in turn applied to determine the most likely defect distribution for a given set of diagnosis results. Figure 2 (next page) shows typical RCD analysis flow.

**Figure 1. Layout-aware scan diagnosis identifies the location and classification of defects in digital semiconductor devices.** Click on image to enlarge.
Figure 2. Root Cause Deconvolution determines the root cause distribution and devices most likely to fail for each root cause. Click on image to enlarge.

Layout-aware diagnosis is performed on a set of die that failed manufacturing test (1). Each diagnosis result contains a set of root causes that are potential explanations for the failure. If we sum all the root causes and count the number of die whose failure could be explained by each root cause, we get a diagram that includes all the real root causes as well as the noise (2). RCD then eliminates this noise and identifies the underlying root cause distribution (3). From this distribution, the user can focus on the most significant root cause, on a root cause that hasn't been seen before, or for other unexpected reasons. Along with the root cause distribution, RCD assigns a probability for root cause per diagnosis suspect (4). This means that the user can easily identify the die that has the highest probability of representing a particular root cause, and use that as way to select die for FA (failure analysis). When comparing the RCD results to the original diagnosis report for one failing die, we see that RCD has eliminated several of the original root causes, thus effectively improved the resolution for that individual result (5). In this particular example, the original report contained seven possible root causes for one failing die, while RCD limited this to one single result. The layout snapshots show the defect bounding boxes before and after RCD (6).

The value of RCD is obvious when analyzing a single collection of fail data, such as a single wafer or a single lot. This technology has also proven useful for longer term yield monitoring. RCD defect distributions for multiple lots and even multiple devices can be compared to identify defect trends and variation. A recent paper published by GLOBALFOUNDRIES stated that "To best leverage RCD, the analysis population needs to be carefully prepared. By accumulating the RCD results across time and designs, helpful yield analysis can be carried out with minimal effort."

In conclusion, diagnosis-driven yield analysis with RCD is a quick and cost effective way to determine the underlying root causes represented in a population of failing devices from test data.
alone. This technology can, for instance, ferret out the final 1% yield loss in mature technologies, thus providing significant value to the yield and failure analysis process at fabless semiconductor companies because the test data is readily available.

References:

Also See
Layout-Aware Diagnosis
A Framework for Logic-Aware Layout Analysis