Latching power switch uses momentary pushbutton

Anthony Smith - January 20, 2014

Low-current, momentary action pushbutton switches, such as PCB-mount ‘tactile’ types, are cheap, and available in an abundance of different styles. Latching types, on the other hand, are often larger, more expensive, and available only in a relatively limited range of styles. This can be a problem if you need a small, inexpensive switch for latching power to a load. The solution is to convert a pushbutton's momentary action into a latching function.

Previous Design Ideas have proposed solutions based on discrete components (Ref. 1) and IC-based circuits (Ref.2 and Ref.3). The circuit outlined below, however, requires just two transistors and a handful of passive components to achieve the same result.

The circuit in Figure 1(a) is configured to latch power to a low-side (ground-referred) load. It works in 'toggle' mode; that is, the first switch closure applies power to the load, the second removes power, and so on.

![Circuit Diagram](image)

**Figure 1** Circuit converts momentary action push switch into latching power switch.

To understand how the circuit operates, assume that the DC power supply, $+V_S$, has just been
applied, capacitor C1 is initially uncharged, and Q1 is off. The P-channel MOSFET, Q2, is held in its off state by R1 and R3, which work in series to pull the gate up to \( +V_s \), such that \( V_{GS} \) is zero. The circuit is now in its 'unlatched' state, where the load voltage, \( V_L \), at the OUT (+) terminal is zero.

If the normally-open push switch is momentarily closed, C1 – being uncharged – pulls Q2’s gate to 0V, thus turning on the MOSFET. The load voltage at OUT (+) now rises immediately toward \( +V_s \), and Q1 receives base bias via R4 and turns on. Under these conditions, Q1 saturates and pulls Q2’s gate low via R3, thus holding the MOSFET on when the switch has opened. The circuit is now in its 'latched' state, where both transistors are on, the load is energized, and C1 charges up to \( +V_s \) via R2.

When the switch is momentarily closed for a second time, the voltage on C1 (by now approximately equal to \( +V_s \)) is transferred to Q2’s gate. Since Q2’s gate-source voltage is now roughly zero, the MOSFET turns off and the load voltage falls to zero. Q1’s base-emitter voltage also falls to zero and the transistor turns off. Therefore, when the switch is released, there is nothing to hold Q2 on, and the circuit reverts to its 'unlatched' state, where both transistors are off, the load is de-energized, and C1 discharges via R2.

Resistor R5 across the output terminals is an optional component that acts as a pull-down. When the switch is released, C1 discharges via R2 into the load. If the load impedance is very high (i.e., similar in magnitude to R2), or if it contains active devices such as LEDs, the load voltage at the instant Q2 turns off may be large enough to bias Q1 on via R4, thereby preventing the circuit from turning off properly. The presence of R5 pulls the OUT (+) terminal down to 0V when Q2 turns off, thus ensuring that Q1 turns off rapidly, and allowing the circuit to revert to its unlatched state in a proper manner.

Provided the transistors are correctly rated, the circuit will work over a wide voltage range and is well suited to driving loads such as relays, solenoids, LEDs, and so on. However, beware that certain DC fans and motors continue to rotate when their drive power is removed. This rotation can generate an EMF large enough to bias Q1 on, thereby preventing the circuit from switching off. You can eliminate this problem by inserting a blocking diode in series with the output, as shown in Figure 1(b). You must also include R5 to ensure Q1 turns off properly.

The complementary circuit outlined in Figure 2 is intended for 'high-side' loads connected to the positive supply rail such as the relay shown in this example.
Figure 2 Complementary circuit intended for high-side loads.

Note that Q1 has been replaced with a PNP transistor, and Q2 is now an N-channel MOSFET. The circuit operates in a similar way to the one described above. Here, R5 acts as a pull-up resistor which pulls the OUT (-) terminal up to +VS when Q2 turns off, thus ensuring that Q1 turns off quickly. As in the previous circuit, R5 is optional and only necessary for the types of load mentioned previously.

Note that in both circuits, the time constant produced by C1-R2 provides for debouncing of the push switch contacts. Normally, a value of 0.25s to 0.5s should be adequate. Smaller time constants may lead to erratic behaviour, whereas a larger time constant increases the waiting time between switch closures necessary to ensure that C1 charges and discharges properly. With C1 = 330nF and R2 = 1MΩ as shown, the time constant is nominally 0.33s. This is usually sufficient to debounce the contacts and to allow the load power to be toggled after a couple of seconds or so.

Both circuits are intended to latch and unlatch in response to brief, momentary switch closures. However, they have each been designed to ensure correct operation even if the push switch is held closed for any length of time. Consider the circuit in Figure 2 when Q2 is on. When the switch is
pressed to unlatch the circuit, the gate is pulled down toward 0V (since C1 is uncharged) and the MOSFET switches off, allowing the junction of R1-R2 to rise toward +V_s via R5 and the load impedance. At the same time, Q1 also switches off, such that Q2's gate is pulled to 0V via the series combination of R3 & R4. If the switch is released immediately, C1 will simply charge up toward +V_s via R2. However, if the switch is kept closed, Q2's gate voltage will be defined by the potential divider formed mainly by R2 and R3+R4. If we assume that the OUT (-) terminal is roughly equal to +V_s when the circuit is unlatched, Q2's gate-source voltage is given by: \( V_{GS} = \frac{ (+V_s) \times (R3 + R4)}{(R2 + R3 + R4)} = 0.02V_s \). Even if +V_s is as high as 30V, the resulting gate-source voltage of around 0.6V will be too low to switch the MOSFET on again. Consequently, both transistors remain off until the switch contacts open.

The circuit in Figure 2 is latched on by momentarily closing the push switch when C1 has charged up to +V_s, which causes OUT (-) to drop to 0V as Q2 immediately turns on, rapidly followed by Q1. A momentary switch closure would allow C1 to discharge to zero via R2 after the contacts open. However, if the switch is held closed, Q2's gate voltage will be defined by the potential divider formed by R2 and R3. Since Q1 is saturated, the junction of R3-R4 at Q1's collector will be pulled up to +V_s, and the junction of R1-R2 will be pulled down to 0V via Q2. Therefore, with the switch held closed, Q2's gate-source voltage is given by: \( V_{GS} = \frac{ (+V_s) \times R2}{(R2 + R3)} = 0.99V_s \). Consequently, provided the supply voltage is at least equal to Q2's gate-source threshold voltage, both Q2 and Q1 will remain on until the switch contacts open.

Both circuits provide an inexpensive way of deriving a latching function from a momentary switch and, just like a mechanical latching switch, the quiescent (unlatched) power dissipation is zero.

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