Minimize crosstalk with optimized PCB routing technique

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I. Introduction

Today, there are a number of high speed digital communication protocols applied in portable computing devices with compact PCB dimensions. Protocols such as PCIe, USB, and SATA have data throughput of gigabits per second and differential amplitudes of hundreds of millivolts. These high speed serial signals require proper routing on a PCB to minimize inter-pair crosstalk that could cause data corruption between the two ends of the channel.

Crosstalk occurs when there is coupling of energy from aggressor signal to victim signal in terms of the interference of electric and magnetic field. Electric field is coupled via mutual capacitance between the signals. On the other hand, magnetic field is coupled via mutual inductance between the signals [1].

The induced voltage and current from the aggressor signal to the victim signal are computed in equation (1) and (2) respectively [1]. Meanwhile, the mutual capacitance and mutual inductance between aggressor and victim are computed in equation (3) and (4) respectively [1] [2].
As shown in equation (1), (2), (3), and (4), inductive and capacitive coupling between the aggressor and victim decreases when distance between them increases. However, large inter-pair air gap is difficult to implement in compact PCBs designed for portable computing devices due to limited routing space.

The problem of crosstalk or coupling can be mitigated by implementing interleaved routing on microstrip and non-interleaved routing on stripline [3].

\[ V_{Lm} = L_m \frac{dI}{dt} \]  \hspace{1cm} (1)

\[ I_{Cm} = C_m \frac{dV}{dt} \]  \hspace{1cm} (2)

\[ C_m = \frac{\varepsilon A}{d} \]  \hspace{1cm} (3)

\[ L_m \approx 2\left(l \times \text{LOG}\left(\frac{2l}{d}\right) \right) - l + d \]  \hspace{1cm} (4)

\( V_{Lm} \) = induced voltage on victim

\( L_m \) = mutual inductance between victim and aggressor

\( \frac{dI}{dt} \) = transient edge rate of current due to aggressor

\( I_{Cm} \) = induced current on victim

\( C_m \) = mutual capacitance between victim and aggressor

\( \varepsilon \) = dielectric permittivity

\( A \) = overlapped conductive area between victim and aggressor

\( d \) = distance between victim and aggressor

\( \frac{dV}{dt} \) = transient edge rate of voltage due to aggressor

Interleaved mode is implemented when FEXT is more significant than NEXT. On the other hand, non-interleaved routing is implemented when NEXT is more significant than FEXT. NEXT refers to the crosstalk of victim’s end near transmitter of aggressor. FEXT refers to the crosstalk of victim’s end near receiver of aggressor. The investigation to compare FEXT and NEXT on microstrip and
stripline is conducted by analyzing the s-parameters and transient response of an aggressor signal and victim signal that are tightly coupled [4].

II. Simulation

The simulation model of s-parameter and transient analysis in ADS are shown in Figure 3 and 4 respectively. In Figure 3, single mode s-parameters of victim and aggressor pairs of 1000 differential impedance and 3 inch length are converted to differential mode mathematically. Port 1 and 2 refer to the input and output ports respectively, of the aggressor pair. Meanwhile, Port 3 and 4 refer to the input and output ports respectively, of the victim pair. The inter-pair air gap between the aggressor and victim is set as 8 mils (1 × the trace width).

In Figure 4, the victim pair is represented by the transmission lines in the middle and terminated with resistors at both ends. Square waves with high edge rates of 30ps are injected into the transmission lines above and below the victim pair, and these two pairs serve as aggressors.

The NEXT is represented by differential s-parameter Sdd31, while FEXT is represented by Sdd41. The notation of Sdd31 is defined as the gain ratio of induced voltage at port 3 (victim's input) with respect to incident voltage at port 1 (aggressor's input). On the other hand, Sdd41 is defined as gain ratio of induced voltage at port 4 (victim's output) with respect to incident voltage at port 1 (aggressor's input).

The simulated s-parameter of the coupled microstrip and stripline pairs are shown in Figure 5 and 6 respectively. In Figure 5, Sdd31 is lower than Sdd41, which indicates that Sdd41 or FEXT has
higher gain compared to Sdd31 or NEXT on microstrip routing. In Figure 6, Sdd31 has higher gain compared to Sdd41 on stripline routing.

The simulated time domain transient response of FEXT and NEXT of the coupled microstrip and stripline pairs are shown in Figure 7 and 8 respectively. With reference to microstrip pairs in Figure 7, when the signals at aggressor lines rise and fall during transient state, the induced voltage spike at the far end (0.3V) is much higher as compared to near end (0.05V) of victim lines. Whereas for stripline pairs in Figure 8, the induced voltage spike at the far end of victim lines is trivial as compared to the interference at the near end (0.05V). The false trigger or induced spike on the victim signal increases the probability of violating the noise margin of its receiver IC, which in turn increases the BER.
In order to minimize the crosstalk between tightly coupled pairs, interleaved routing shall be implemented on microstrip, versus non-interleaved routing on stripline.

III. Measurement on prototype PCB

In order to correlate the simulation result with practical measurement, a prototype PCB was fabricated. The measured s-parameters of the coupled microstrip and stripline pairs are shown in Figures 9 and 10 respectively. With reference to Figure 9, NEXT has lower magnitude as compared to FEXT. Meanwhile, in Figure 10, FEXT has lower magnitude as compared to NEXT.
The measured time domain transient response of FEXT and NEXT of the coupled microstrip and stripline pairs are shown in Figures 11 and 12 respectively. With reference to microstrip pairs in Figure 11, when the signals at aggressor lines rise and fall during transient state, the induced voltage spike at the far end (0.3V) is much higher than the near end (0.1V) of victim lines. Whereas for stripline pairs in Figure 12, the induced voltage spike at the far end of victim lines is trivial as compared to the interference at the near end (0.1V).
IV. Conclusion

The technique of optimized signal routing to minimize crosstalk is studied in this paper. Analysis results of s-parameter and time domain transient response show that crosstalk is minimized if interleaved routing is implemented on microstrip, and non-interleaved routing on stripline. In PCB designs that implement high data rates, optimized routing must be taken into consideration to guarantee excellent signal quality performance.

Chang Fei Yee has been working at Keysight since 2006, with experience in digital board design, high speed backplane design, and signal & power integrity analysis.
References:

[1] Crosstalk overview by Intel


[4] Use S-parameters to describe crosstalk, Eric Bogatin and Alan Blankman