**Boundary scan: Seven benefits**

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**Boundary Scan: What Is It?**

Boundary scan test techniques were first discussed in the late 1980s. At the time, experts believed that the growing complexity of chips would have a serious effect on an ICT system’s ability to place a nail accurately on a test pad. In addition, the development of multi-layer boards compounded the problem of physical access for testing interconnects between devices on a PCB.

Many of the testing industry experts predicted that the “bed of nails“ test system would disappear with the increasing complexity of chips. As a result, a group of concerned test engineers banded together to address this problem. The group was known as the Joint Test Action Group (JTAG). Their preferred solution was to access device pins by means of an internal serial shift register around the boundary of the device as shown below. In the boundary scan design, the chip’s IOs were supplemented with the boundary scan cell (a storage element). The collection of boundary scan cells on a board can be configured in various ways to achieve a parallel-in, parallel-out shift register that is used for testing and for on-board programming purposes.

![Figure 1](image)

**Figure 1** IC including Boundary Scan Test Control

At the device level, the boundary scan elements are independent of the functionality of the device,
but the scan path provides virtual access to devices for testing and programming. In fact, boundary scan interconnect tests will verify the presence, orientation and correct bonding of devices – a functionality similar to ICT but without the physical access. Essentially, boundary scan cells can be thought of as a set of virtual nails with the ability to set up and apply tests across the interconnect structures on a board. Increasingly, manufacturers are finding that boundary scan can reduce costs and increase test and manufacturing efficiency.

Benefits of Boundary Scan

Reusable Test Vectors

The cost of test generation can be reduced with JTAG. At the board level, boundary scan testing provides the equivalent of in-circuit testing without the expense and complexity of a bed-of-nails fixture. The JTAG technique can allow the reuse of test patterns at various levels of hierarchy from chip-level to board-level and board-level to system-level. For example, at the board-level, a portion or a full set of chip level test vectors can be reused as a nucleus for the board-level test.

Reduced Test Time

Another benefit of a boundary scan system is the possibility of reducing test time, particularly in the diagnostic area. The boundary scan technique may take higher time in loading and unloading of the test stimuli and circuit responses from the boundary scan chain. If we assume a complex design (with the required level of ‘single stuck-at’ fault coverage as 99%), the boundary scan test time might be much shorter. This is because of the divide-and-conquer approach used.

Reduced Time to Market

Use of JTAG technique at the chip level and board level can have a significant positive impact on time to market. This is because test generation is faster and easier. Generally, significant amounts of effort are required to develop an in-circuit test module for a new IC. This task can now be completed in a matter of hours because it is no longer necessary for the board test engineer to understand the detailed operation of the new chip.

In highly competitive markets, time-to-market is a matter of survival. For EMS (Electronic Manufacturing Service providers) and OEM (Original Equipment Manufacturers), the JTAG technique would generate tremendous business value. The boundary scan technique can reduce a system's time-to-market during every phase of the life cycle, beginning with prototype test and continuing in manufacturing and functional test.

Faster ROI

Boundary scan test systems are relatively economical when compared to the In-Circuit Test (ICT) system. Hence, the EMS can surpass the investment in the boundary scan test equipment, once they get new test projects. This way, the JTAG test system can provide the new area of opportunity to service a new business. As a result, the break-even for investments into JTAG systems is much faster for EMS companies.

Reduced Design Iterations

During the prototype phase, designs typically are not stable enough for OEMs to invest in ICT
fixtures. If manufacturers can verify the structural integrity of the design, then OEMs will be able to bring up boards faster, with higher yields and at reduced expenses.

**Efficient and Economical Production**

If EMS companies were to switch from ICT to JTAG test systems, this would increase test coverage and reduce costs, because JTAG test systems require fewer test points compared to ICT. The JTAG test system can also take on more of the test load, and improve the overall quality and yield. This results in an increase of the production output. We have come across instances where companies have eliminated two thirds of their test points, and have saved about $50,000 per test fixture.

**Functional Test**

Diagnosing structural failures using the functional test is difficult compared to the boundary scan test technique. Switching from ICT to JTAG test systems will significantly reduce test time. Additionally, accessing on-board processors for emulation through boundary scan reduces the time that boards spend in functional testing. It also lowers the possibility of faults introduced from the added physical handling that other methods of processor access require. The diagnostic abilities of boundary scan test environments can quickly isolate faults down to the level of a particular pin.

Furthermore, since IEEE 1149.1 establishes a common four- (or five-) pin interface and protocol with the tester, such commonality across all board types will save even more in fixture or interface adapter costs, particularly if one considers the cost impact of engineering changes.

**Challenges with Boundary Scan**

**Area Overhead / Additional Circuits**

The first and most obvious penalty of including boundary scan capabilities is the cost of the additional circuitry. The effect on circuit size of adding boundary scan capabilities is difficult to predict. Predicting boundary scan capabilities on circuit size is difficult because much depends on the detail of the implementation. For example: Are "holding" registers or latches provided in all boundary scan cells? What is the geometry and positioning of the cells? Are they providing user defined instruction registers? What is the size of the instruction register? How many IO pins are there on the chip?

The following examples provide estimates for the overall size of the circuitry required to give conformance to IEEE 1149.1.
Take a full-custom 6mm × 6mm IC built in a 2.0 micron single-layer metal CMOS process. Implementation of the TAP (Test Access Port) controller requires about 80 NAND gates. A more efficient implementation could, however, be achieved using a transistor level state machine design. An initial implementation in the stated technology requires a silicon area of approximately 0.3 mm$^2$.

An instruction register containing two bits (the minimum configuration) would occupy on the order of 0.02 mm$^2$. The bypass register is approximately one half of the size of the minimum instruction register, or 0.01 mm$^2$.

An estimate of the total size of the boundary scan register can be obtained by looking at the size of the boundary scan cell for an output pin illustrated in figure given below. A circuit that implements this design requires around 0.015 mm$^2$. It can be expected that boundary scan cells for input and other pin types would be of similar size. Therefore, for an IC with 40 system pins, boundary scan registers would require 0.6 mm$^2$.

The combined silicon area for a minimal implementation comprising a TAP controller, a two-bit instruction register, a bypass register, and a 40-bit boundary scan register would be approximately 1 mm$^2$ from the above figures (including a small allowance for the multiplexers, etc., required to complete the minimum implementation of IEEE 1149.1). This represents an increase in size of 3% for the 36 mm$^2$ IC.

### Additional Pins

The second most apparent penalty is the need to add dedicated test pins to the chip. IEEE Std. 1149.1 calls for a minimum of four pins. While the fifth test logic reset (TRST*) pin is optional, feedback from some IC manufacturers indicates that they may also provide this pin. The TAP can access many testability features within a design that might otherwise require package pins for additional data or control access. The four or five pins required by the TAP may therefore frequently provide for all test purposes. Viewed in this way, the requirement for a number pins dedicated to test is not unusual — many ICs today use several dedicated test pins to allow them to be tested economically.
Higher Design Effort

Since there is additional circuitry associated with boundary scan, it can be safely assumed that some form of additional design effort will be required. Application-specific ICs (ASICs) are being developed that have the boundary scan path built into the periphery of the base logic array.

Performance Degradation

Performance is another consideration. The multiplexer that feeds the system pin could add two gate delays. Combined with the additional delay due to the input loading, the propagation delay of signals leaving the chip would increase. Similarly, the delays experienced by signals entering the chip would increase if boundary scan cells that include multiplexers in the pin-to-logic data path are used. The importance of these additional delays clearly depends on the application for which the chip is intended.

It must be pointed out that the use of multiplexers at output pins to permit observation of test data from the core of the design is already commonplace. Many ASIC companies require that complex macro-cells are connected in this way to ensure that test stimuli can be applied. After considering this situation, we can say that there is no additional delay introduced by the inclusion of a boundary scan path. The multiplexer at the output needs to be widened to allow for the input from the boundary scan shift-register stage.

Power Consumption

As circuits are added to the basic design, an increase in the power consumption of the component is expected. For CMOS IC designs, the increase in consumption during normal operation will be small because the boundary scan path and much of the other test logic will be inactive. Only the TAP controller will remain active since, in the absence of a TRST* input, it must continue to be clocked with the test mode select (TMS) input. TMS should be driven to logic 1 to ensure that the controller can return to the Test—Logic—Reset state following any upset.

Implementation Considerations

There are list of design rules which describe the limitations of an In-Circuit Test system (ICT) compared to JTAG test system.

ICT Design Rules

- 0.00196 square inch per test point
- 1,000 test points means 2 square inches lost area on the PCB
- Provide keep-aways (protected area) around test points for tall components
- Keep test points away from board edge
- Avoid probing both sides of the board
- Avoid moving test points after the fixture has been constructed
Additional Benefits of JTAG over ICT: Boundary scan saves space:

- Save 2 square inches for every 1,000 test points eliminated
- Traces no longer needed to the test points

The additional benefits of JTAG over the ICT will be considered as a trade off between the area overhead due to additional circuitry, and test points elimination.

Conclusion

In short, the boundary scan technique has both positive and negative impacts at the board and system level test. Boundary scan is economical as it speeds up the test process, ensuring higher yields from manufacturing and many other cost-saving measures. It can generate additional solutions for the EMS by expanding into new areas like functional test. Alongside of all these advantages, boundary scan has two major drawbacks: area overhead, and additional design effort. After comparing the ICT system requirements of test points and fixtures, boundary scan still manages to balance its area overhead and design efforts.

Today, with increasing die sizes and shrinking technology nodes, JTAG has manifold benefits over ICT testing. This advantage increases with the increasing complexity and size of the IC. We have realized significant gains with designs of over 30 million gates and 10 million scan cells at 28nm technology using JTAG.

Also see:

- Boundary scan goes underground
- Boundary Scan Tutorial
- PCB test: nails or TAP?
- Boundary-scan tips pay board-test dividends