CMOS 3-11GHz UWB LNA employs current-reuse

Sichun Du, Hongxia Yin, Xiangyue Shi, Wenbin Huang - June 05, 2014

Abstract: An ultra-wideband LNA utilizing current-reuse configuration is presented in this paper. With the current-reuse configuration as the input stage, the broadband input matching network has good reflected coefficient and the power dissipation of the whole circuit is greatly suppressed. The simulation is based on CHRT 0.18µm mixed signal/RF CMOS process. The LNA exhibits the forward power gain (S21) of 12dB to 14dB and the input and output reflection coefficient lower than -9 dB, along with a noise figure (NF) ranging between 2.45 and 3.8dB over a 3.1~10.6GHz.

I. Introduction

Ultra Wide Band (UWB) technology refers to equipment working at 3.1 to 10.6 GHz frequency. Because UWB technology has lots of advantages such as high data rate, low cost and low power dissipation [1], it has wide applications in wireless personal area network, medical-image systems, and vehicular communications. In UWB wireless communication system, the RF transceiver is the most important part which contains LNA, Mixer and so on.

The design of the traditional narrow-band LNA faces many challenges such as input impedance match, voltage gain, noise figure and power consumption. Besides these targets, the UWB LNA should also pay attention to the linearity and the flatness of the gain [2], because the UWB system would easily suffer from the in-band interferences from other systems.

Up to now, several techniques have been reported to improve high performance in designing UWB LNA. A distributed amplifier is proposed in reference [3]. It can absorb the parasitic capacitance and provide good matching and linearity, but the power consumption and the chip area are quite high; In [4], a filtering is adopted to achieve wideband input matching, this topology can reduce power and improves the linearity, but it occupies a big area and deteriorates noise performance at a low-frequency band. A resistive shunt feedback is used in UWB LNA [5]. Although this circuit achieves the wideband performance by the feedback configuration, it is hard to satisfy gain and noise requirements simultaneously due to the additional resistance and inherent capacitance of the transistor. A differential UWB CG-LNA employs capacitive cross-coupling to reduce the NF [6], but this cross-coupling add the quality factor of the parallel RLC input network, reducing the matching BW.

In this study, a different UWB LNA is proposed, which adopts a current-reused topology as the input matching network, as well as the current mirror output stage. Because of the current-reuse input network, the whole circuit has a good reflected coefficient in the whole bandwidth and its power dissipation is greatly suppressed. And the current mirror buffer can provide enough gain. This UWB
LNA is particularly suitable for the limited power supply condition.

II. Circuit Topology and Analysis

The schematic of the proposed UWB LNA is shown in Fig.1. The circuit is made up of three stages. The first stage adopts current-reused structure in order to reduce the power dissipation [7]. M1 and M2 are complementary devices and use the common biased current. L3-L6 are used to neutralize the effect of the parasitic parameters to expand the bandwidth. The cascode amplifier as the second stage provides enough voltage gain and isolation. We also add L7 and R2 into the circuit for getting the flat gain because the inductor peaking impedance increases with increasing of the operating frequency. The current mirror M5, M6, C3, R3, L8 works as an output buffer.

![Fig.1 the proposed UWB LNA topology](image)

1. Wideband Matching Design

In order to cover the 7.5GHz bandwidth, this LNA adopts the LC pass-band filter as the input matching network. These components C1, L1, L2 including the source degeneration inductor L6, L3 compose the LC ladder filter. It can absorb the parasitic capacitance as a part of the filter so that it can reach the good input reflection coefficient within the whole bandwidth. The input impedance of the first stage is given in Fig.2.
$C_{gs}$ is the parasitic gate-to-source capacitance. $L_s$ is the equivalent inductor of the two source degeneration inductor ($L_3, L_6$), $L_0$ is the equivalent inductor of $L_4$ and $L_5$. For simplicity, all other parasitic and body effects are ignored. When the circuit is in resonance, the input impedance $R_{in}$ can be derived as:

$$R_{in} = \frac{R_1 + R_{load}}{1 + g_m R_{load}}, \quad (g_m = g_s + g_p)$$

(1)

So we can set the parameters $R_1$ and $g_m$ to improve the input impedance match easily.

2. Current-Reused Technique

The traditional topology of LNA usually uses the Cascode amplifier as the input part. However, the Cascode amplifier has two stacks of the NMOS transistors, it is not suitable for the low supply voltage. So the current-reused structure is adopted in this design. As shown in Fig.3, this current-reused structure is composed of PMOS and NMOS. They use the same bias current. This method not only can decrease the supply voltage but also reduce the power dissipation. The equivalent transconductance of the current-reused topology is the sum of the two transistors.
The minimum supply voltage, keeping both PMOS and NMOS transistors in saturation region, is

$$V_{DD_{\text{min}}} = \sqrt{\frac{2L_p I_D}{\mu C_{ox} W_p}} + |V_{tp}|$$  \hspace{1cm} (2)

In order to flatten the gain, we add the inductors (L3 L4 L5 L6) to the circuit. They can resonate with the capacitance and compensate the effect of the parasite parameters.

3. Current Mirror Buffer

The buffer is consisted of M5, M6, R3, C3 and L8. The transistors M5, M6 compose a current mirror. The C3 and L8 in parallel would resonate at the working frequency. They can select the useful signal. The gain of the buffer is based on the proportional relationship of the width of the transistors in current mirror.

As known, the drain current of the transistor M5, M6 can be derived as follows. For simplicity, Channel length modulation effect is ignored.

$$i_5 = \frac{1}{2} \mu C_{ox} \frac{W_5}{L_{\text{min}}} (V_{gs5} - V_{th})^2$$  \hspace{1cm} (3)

Where $i_5$ is the drain current of transistor M5, $V_{gs5}$ is the gate-source voltage of transistor M5, $W_5$ is the width of transistor M5
Where $i_6$ is the drain current of transistor M6, $V_{gs6}$ is the gate-source voltage of transistor M6, $W_6$ is the width of transistor M6.

By (4)/(3), (5) can be obtained:

$$\frac{i_6}{i_5} = \frac{W_6}{W_5}$$  \hspace{1cm} (5)

If $W_6 > W_5$, the current mirror can amplify the current signal. Enough voltage gain can be gotten by adjusting the width of the transistors.

**Simulation results**

**III. Simulation Result**

The simulation in Cadence Spectre proves that this UWB LNA has good performances. The supply voltage of this UWB LNA is 1.5V. Shown in fig.3, the input return loss (S11) in the whole bandwidth is lower than -9 dB. Fig.4 indicates the output return loss (S22) is less than -10dB. The S11/S22 proves the UWB LNA has achieved good input/output matching over the whole bandwidth. The noise figure is decided by the first stage, current-reuse stage. Both NMOS and PMOS are resized to decrease the noise figure. The lowest NF can reach 2.4dB in Fig.5. Fig.6 shows the reverse isolation (S12) of the UWB LNA. The S12 is less than -60 in the picture. Fig.7 illustrates the LNA achieves 10~14 dB voltage gain. The voltage gain is flat because of adding L7 and R2 into the circuit.

![S-Parameter Response](image)

Fig.4 Input Return Loss (S11)
Table.1 Performance Summary and Comparison With Published Works

<table>
<thead>
<tr>
<th>Specification</th>
<th>This Work</th>
<th>[8]</th>
<th>[9]</th>
<th>[10]</th>
<th>[11]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.18μm CMOS</td>
<td>0.18μm CMOS</td>
<td>0.13μm CMOS</td>
<td>0.13μm CMOS</td>
<td>0.18μm CMOS</td>
</tr>
<tr>
<td>Bandwidth(GHz)</td>
<td>3.1~10.6</td>
<td>3.1~10.6</td>
<td>2~9</td>
<td>2.3~9.3</td>
<td>2~4.6</td>
</tr>
<tr>
<td>Input Return Loss(dB)</td>
<td>&lt;-9</td>
<td>&lt;-8</td>
<td>&lt;-10</td>
<td>&lt;-9.9</td>
<td>&lt;-10</td>
</tr>
<tr>
<td>Reverse Isolation(dB)</td>
<td>&lt;-59</td>
<td>&lt;40</td>
<td>-</td>
<td>-</td>
<td>&lt;50</td>
</tr>
<tr>
<td>Voltage Gain(dB)</td>
<td>10~14</td>
<td>13.5~15</td>
<td>11.4~11.6</td>
<td>6.3~9.3</td>
<td>9.5~10.1</td>
</tr>
<tr>
<td>Output Return Loss(dB)</td>
<td>&lt;-8.5</td>
<td>-</td>
<td>&lt;-10</td>
<td>&lt;-13</td>
<td>&lt;-10</td>
</tr>
<tr>
<td>Noise Figure(dB)</td>
<td>2.45~3.8</td>
<td>3.1~6</td>
<td>4.45~9</td>
<td>4~9</td>
<td>2.3~6</td>
</tr>
</tbody>
</table>

IV. Conclusion

A CMOS ultra-wide bandwidth low-noise amplifier using current-reused configuration is proposed in this paper. The simulation results show that the proposed UWB LNA gives 14 dB maximum voltage gain between 3.1GHz to 10.6GHz with the minimum 2.45dB noise figure from the 1.5 V power supply. The input and output return loss are both less than -8 dB, that proves the good input/output matching of the whole circuit.
V. Acknowledgements

The authors would like to thank the Open Fund Project of Key Laboratory (No. 13K014), Young Teachers Program in Hunan Universities and The Science for financially supporting this research.

VI. References


Also see:

- Novel low-power high-gain CMOS LNA for UWB receivers