Novel low-power high-gain CMOS LNA for UWB receivers

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Abstract: This paper presents a highly linear low power and high gain CMOS common-gate (CG) LNA for UWB receivers. The proposed LNA uses current-reuse, forward-body biasing, and shunt-series peaking techniques. The current-reuse and forward-body biasing techniques are adopted in order to reduce power consumption while achieving reasonable power gain. In addition, the proposed CG architecture LNA with a shunt-series peaking technique can easily obtain wide bandwidth. The proposed LNA circuit is designed and simulated in 0.18µm RF CMOS process. Simulation results of the proposed LNA achieves from 16.5 to 18.2dB gain ($S_{21}$) over 3-11GHz bandwidth, a minimum noise figure (NF) of 2.1dB, and an input third order intercept point (IIP3) of 10dBm, while consuming 3.1mW from a 1.3V supply voltage.

1. Introduction

In February 2002, the Federal Communications commission (FCC) has allocated 7,500 MHz of spectrum for unlicensed use of ultra-wideband devices in the 3.1 to 10.6GHz frequency band[1]. The benefits that UWB technology can provide, including low power, high data rates (up to 1 Gb/s), low cost and reduced interference. Being the first block of the UWB receiver, the UWB low-noise amplifier (LNA) plays a crucial role in amplifying the received signal while adding little noise to it. The UWB LNA must meet several stringent requirements, such as broadband input matching, flat and high power gain, low noise figure (NF), high linearity and low power consumption, which directly affect characteristics of the whole UWB receiver.

Up to now, a number of UWB LNAs based on CMOS technology have been developed in literature[2-8]. The distributed amplifier (DA) is one of the most popular architectures for the wideband LNA design. Because DA LNAs provide good wideband input matching, flat gain over a wide range of frequencies, and generally higher IIP3 [2], [3], [4]. However, the DA LNA consumes a great deal of power, occupies a large chip area, and its power gain is quite low. Resistive feedback is a good solution for obtaining wide bandwidth and flat power gain [5], [6], [7]. However, the use of a resistor in the feedback path reduces the power gain and degrades the noise performance. Recently, a new topology in the LNA design is the cascode with a Chebyshev input matching filter, which provides good wideband input matching and high power gain [8]; however, the noise figure (NF) is degraded by the insertion loss of the filter.

A big challenge for designing UWB LNAs is the stringent linearity requirement over a wide frequency range, due to the large numbers of in-band interferences in UWB system, and the cross-modulation/inter-modulation caused by blockers or transmitter leakage [9] in a reconfigurable receiver. Furthermore, while transit frequency($f_t$) increases with technology scaling, linearity worsens due to lower supply voltage and high-field mobility effects[9]. Therefore, wideband
linearization technique is a research hotspot. A linearization approach for high-frequency wideband applications is desired. Up to now, several techniques have been proposed to improve the linearity of LNA circuit. The optimal biasing technique [10], [11], which optimizing the overdrive voltage ($V_{gs}-V_{th}$), can be used to achieve a peak in IIP3. However, the bias voltage range for IIP3 peak is very narrow, making the linearity boosting very sensitive to process variation. The derivative super-position (DS) method [12-14] uses an additional transistor’s nonlinearity to cancel that of the main device; it involves MOS transistors working in triode [12] or weak inversion region [13], [14]; therefore, the DS method is difficult to match the transistors working in different regions, resulting in a linearity improvement highly sensitive to pressure-volume-temperature (PVT) variations. The body biasing technique [15] is suitable to improve the linearity performance, however, it degrades the gain and noise performances. In [16], the post-distortion technique is utilized to improve the linearity. Owing to all transistors in saturation region and also avoids the input matching degradation; this technique has a robust increase of linearity.

In this paper, a highly linear, low power UWB CG-LNA is proposed. Common-gate (CG) LNAs have become more and more popular for UWB systems thanks to their simpler input matching network, better linearity, lower power consumption and better input-output isolation compared with common-source (CS) LNAs. However, as we all know, the power gain of the CG LNA is insufficient [17], so a CS amplifier is utilized as a second stage. The proposed LNA circuit utilizes current-reuse and forward body biasing techniques in order to achieve low power consumption. In addition, shunt-series peaking techniques are used to extend the 3dB frequency bandwidth. Meanwhile, a post-distortion technique is employed to improve the linearity performance of the proposed LNA.

This paper is organized as follows. Section 2 begins with input stage analysis of LNAs and compares the pros and cons of conventional CS and CG topologies. The techniques, which employed to the proposed LNA, are also described carefully in section 2. Section 3 presents the final schematic of the proposed LNA, a gain analysis, a noise analysis, a linearity analysis. Simulation results are shown and compared with other reported LNAs in section 4. Finally, concluding remarks are provided in section 5.

Proposed UWB CG LNA design

2. Proposed UWB CG LNA design

2.1 Input stage analysis

Based on the input matching characteristics, the published CMOS UWB LNA architectures can be divided into two major groups, the common source (CS) and common gate (CG) LNA[18]. General topology of these architectures is shown in Fig.1. Fig.1(a) shows a conventional CS low noise amplifier (LNA) that requires at least two inductors ($L_g$, $L_s$) for simultaneous noise and input matching (SNIM). As we know, the input matching network of the CS low noise amplifier has series resonance. Assuming that the channel resistance $\gamma$, and the gate-drain parasitic capacitance $C_{gd}$ are negligible, respectively, the quality factor (Q) of the CS LNA can be derived as
Where \( \omega_0 \), \( g_m \), \( L_g \), \( L_s \) and \( C_{gs} \) represent the resonant angular frequency of the input impedance, the transconductance of the metal-oxide semiconductor field-effect transistor (MOSFET), the gate inductor, the source inductor and the gate-source parasitic capacitance, respectively. This architecture is inherently narrowband because of the high \( Q \) value and achieving wideband input match to the signal source in the presence of the parasitic capacitances is quite difficult.

Fig. 1 (b) shows a typical CG LNA. The input matching network of the CG LNA has a parallel resonance. The \( Q \) of the CG LNA can be expressed as

\[
Q_{CS} = \frac{1}{\omega_0 g_m L_s}
\]  \hspace{1cm} (1)

\[
\omega_0 = \frac{1}{\sqrt{(L_g + L_i)C_{gs}}}
\]  \hspace{1cm} (2)

Substituting (2) into (1) yields

\[
Q_{CS} = \frac{\sqrt{(L_g + L_i)C_{gs}}}{g_m L_s}
\]  \hspace{1cm} (3)

Where \( \omega_0 \), \( g_m \), \( L_g \), \( L_s \) and \( C_{gs} \) represent the resonant angular frequency of the input impedance, the transconductance of the metal-oxide semiconductor field-effect transistor (MOSFET), the gate inductor, the source inductor and the gate-source parasitic capacitance, respectively. This architecture is inherently narrowband because of the high \( Q \) value and achieving wideband input match to the signal source in the presence of the parasitic capacitances is quite difficult.

Fig. 1 (b) shows a typical CG LNA. The input matching network of the CG LNA has a parallel resonance. The \( Q \) of the CG LNA can be expressed as

\[
Q_{CG} = \omega_0 \frac{C_{gs}}{g_m}
\]  \hspace{1cm} (4)

\[
\omega_0 = \frac{1}{\sqrt{L_s C_{gs}}}
\]  \hspace{1cm} (5)

By substituting (5) into (4), the \( Q_{CG} \) can be re-expressed as

\[
Q_{CG} = \frac{C_{gs}}{g_m \sqrt{L_s C_{gs}}}
\]  \hspace{1cm} (6)

Since \( L_s \) is intended to block the RF leakage to the ground, the \( L_s \) value of the conventional CG LNA is higher than that of the CS LNA. So \( Q_{cs} \) value is higher than \( Q_{cs} \) value. Also, obtaining wideband input match and absorbing parasitic capacitances is relatively simple and is less effected by process variations in the case of the CG topology. To sum up, the CG LNA is a suitable topology for wideband input matching.
Portable applications such as WLAN transceivers, cell phones and sensor networks have to meet stringent performance requirements with the lowest power consumption to preserve battery life. The most efficient approach for reducing power consumption is through power supply voltage scaling. In the proposed LNA circuit, the forward body biasing technique is employed to further reduce the threshold voltage ($V_{th}$), the threshold voltage of MOSFET is well known as:

$$V_{th} = V_{th0} + \gamma(\sqrt{2\varphi_f} - V_{bs} - \sqrt{2\varphi_f})$$

where $V_{th0}$ is the threshold voltage when $V_{bs}$=0, $\gamma$ is the body-effect coefficient, $\varphi_f$ is the surface potential, $V_{bs}$ is the voltage between body and source. Usually, $V_{bs} \leq 0$, so $V_{th} \geq V_{th0}$. In order to reduce the $V_{th}$, we let $V_{bs} > 0$, so $V_{th} < V_{th0}$. The typical value of $V_{th}$ is about 0.5 V, in the proposed LNA, $V_{bs}$=0.29V, $V_{th}$=0.43V.
Circuit Design and Analysis

3. Circuit Design and Analysis

The LNA was designed and simulated in 0.18µm RF CMOS process. Fig. 3 presents the schematic of the proposed LNA including the output buffer (M₄, M₅). The current-reused configuration can be considered as a two stage cascade amplifier, where the first stage is the CG amplifier (M₁), and the second stage is the CS amplifier (M₂). The signal amplified by M₁ is coupled to the gate of M₂ by series resonant (Lᵣ and Cᵣ) while the source of M₂ is bypassed by Cᵦ. Besides, Cᵦ determines the low frequency band expansion and gain flatness. The circuit saves power through the reuse of the bias current. As we know, the power gain of the CG topology LNA is low, so a CS amplifier with gain peaking technique which consists of Rᵢ, Lᵢ, M₂ and Lᵣ is employed in the second stage. To reduce the threshold voltage of the transistor, the forward body biasing technique is employed to this design. The post-distortion technique is utilized in the first stage (M₃), reducing the nonlinearity of the main device (M₁). The circuit parameters of the proposed LNA are summarized in Table I.

<table>
<thead>
<tr>
<th>Devices</th>
<th>Design values</th>
</tr>
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<tr>
<td>M₁</td>
<td>124 µm/0.18 µm</td>
</tr>
<tr>
<td>M₂</td>
<td>48 µm/0.18 µm</td>
</tr>
<tr>
<td>M₃</td>
<td>25 µm/0.18 µm</td>
</tr>
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</table>
### Input Matching

Most RF instruments and coaxial cables have standard impedances of 50Ω, thus the input stage of the amplifier is required to match to 50Ω to have no power reflection [21]. For simplicity, body effect is ignored. The CG input stage of the proposed LNA is shown in Fig.4. The input impedance can be derived as

\[
Z_{in}(\omega) = \frac{1}{g_{m1} + \frac{1 - \omega^2 L_s C_{gs1}}{j\omega L_s} + \frac{(1 - g_{m1} Z_L) + j\omega Z_L C_{in}}{(r_{in} + Z_L) + j\omega r_{in} Z_L C_{in}}}
\]

(16)

where \(C_{ta}\) and \(C_{tb}\) are the total capacitance at node a and node b, respectively. \(g_{ps1}, g_{m1}, \) and \(r_{in}\) are the gate-to-source capacitance, the transconductance, and the output resistance of \(M_1\), respectively. \(Z_L\) is the CS stage equivalent load impedance. As (16) indicates, the input impedance approximates \(1/g_{m1}\) over the frequency band of interest. Because \(g_{m3} \ll g_{m2}\) (\(g_{m2}\) and \(g_{m3}\) are the transconductance of transistor \(M_2\) and \(M_3\), respectively.) the input impedance \(Z_{in}(\omega)\) seen from \(R_s\) of the CG LNA is about the same with and without transistor \(M_3\) present. Therefore, \(M_3\) does not significantly affect input matching. However, for a wideband input match, (16) indicated that \(g_{m1}\) of \(M_1\) in the CG stage should slightly exceed 20mS. Through simulation, we see that the input matching is good when \(g_{m1}\) approaches to 26mS.

The achievable maximum power gain also depends on the output impedance matching. In the proposed LNA, a simple source follower, which consists of \(M_4\) and \(M_5\), is employed to obtain output impedance matching.
3.2 Gain Analysis

If the source of $M_2$ is perfectly grounded by $C_w$, the equivalent schematic of the proposed LNA can be redrawn in Fig.5. As we can see from Fig.5, the proposed LNA is created by the two-stage amplifier. The first stage is a CG amplifier and the second stage is a CS amplifier. For simplicity, the body effect is not considered. The voltage gain of the first stage $A_{v1}$ can be expressed as (17).
\[ A_{V1} = \frac{V_{g2}}{V_{s}} = \frac{g_{m1}Z_s(Z_s + R_s)(1 + g_{m1}Z_s)}{(Z_s + R_s(1 + g_{m1}Z_s))(1 + sC_{d1}Z_s)} \] (17)

where

\[ Z_s = sL_s P \frac{1}{sC_{s1}} \] (18)

\[ Z_d = sL_d PZ_3 P \frac{1}{sC_d} \] (19)

\[ Z_g = sL_g + \frac{1}{sC_g} \] (20)

\[ Z_t = Z_d P(Z_g + \frac{1}{sC_{L1}}) \] (21)

g_{m1}, r_{o1}, R_s, C_{s1}, C_{d1} and Z_3 are the transconductance of M_1, the channel resistance of M_1, the input source resistance (Rs=50Ω), the source parasitic capacitance, which caused by C_{gs1} (the gate-t-source parasitic capacitor of M_1) and the drain parasitic capacitance, which caused by C_{gd1} (the gate-to-drain parasitic capacitor of M_1), the equivalent impedance of M_3, respectively. In addition, \( C_{L1} \) is the parasitic load capacitance of the second stage. Here, the direct current (DC) blocking capacitors (\( C_{in} \) and \( C_{out} \)) are ignored for simplification.

The voltage gain of the second stage \( A_{V2} \) is given by (22).

\[ A_{V2} = \frac{V_{out}}{V_{g2}} = \frac{-g_{m2}Z_{out2}}{1 + s^2L_pC_{L2}} \] (22)

where

\[ Z_{out2} = r_{o2} PZ_L P(sL_p + \frac{1}{sC_{L2}}) \] (23)

\[ Z_L = (R_L + sL_p) P \frac{1}{sC_{d2}} \] (24)

g_{m2}, r_{o2}, C_{L2} are the transconductance of M_2, the channel resistance of M_2, the total loaded capacitance at the second stage output, respectively. Additionally, \( C_{d2} \) is the calculated parasitic capacitance at the drain of M_2, which is produced by the gate-to-drain parasitic capacitor (\( C_{gd2} \)). The overall circuit frequency response of \( S_{21} \) has a great flatness and a higher power gain because of the cascaded combination of the first and second stage. This will be reflected in section 4.
3.3 Noise Analysis

The first stage of a receiver is typically a low noise amplifier and its noise figure is critical to the whole receiver circuit. For simplicity, the parasitic effects, body effects and the influence of $M_3$ to the noise performance are ignored. In the proposed LNA, the mean square noise voltage and the mean square noise current can be expressed as

\begin{align}
\overline{V^2_{n1}} &= 4kTR_1\Delta f \\
\overline{i^2_{n1}} &= 4kT\gamma g_{n1}\Delta f \\
\overline{i^2_{n2}} &= 4kT\gamma g_{n2}\Delta f \\
\overline{i^2_{nR}} &= 4kT / R_L\Delta f
\end{align}

(25) (26) (27) (28)

Which are produced by the source resistor $R_s$, the channel noise of $M_1$, $M_2$ and the load resistor $R_L$, respectively. $k$, $T$, $\gamma$ and $\Delta f$ are Boltzmann’s constant, the absolute temperature in degree Kelvin, the thermal noise coefficient having a value from 1 to 2 in saturation region of a short channel Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) and the noise bandwidth in hertz, respectively.

The noise factor of the proposed LNA can be expressed as (29)
\[ F = \frac{V_{n,\text{out}}^2}{(A_v)^2} \times \frac{1}{V_{nS}^2} \]
\[ \approx 1 + \frac{1}{(A_{v1})^2 R_L} \times \left( \frac{Z_L}{1 + sC_{L1}} \right)^2 \gamma g_{m1} + \gamma g_{m2} + \gamma g_{n2}^2 (R_L + sL_L) \]  

(29)

Where \( V_{n,\text{out}}^2 \) is the total noise at the output and \( A_v \) is the total voltage gain. The total voltage gain \( A_v \) can be obtained by (17) and (22). From (29) we can see the effects of \( g_{m1} \) and \( g_{m2} \) for achieving a lower noise factor. In order to obtain a low noise factor and a low power consumption, \( g_{m1} \) should be a low value. However, on the contrary, this would adversely affects the total noise factor because a low \( g_{m1} \) value would lead to the gain of the first stage is to be low. Alternatively, from (29) we also find that a high \( g_{m2} \) value is beneficial for achieving a low noise factor. However, this increases the power dissipation. Therefore, it is necessary to optimize \( g_{m1} \) and \( g_{m2} \). Because both transconductances depend on transistor width (\( W_1 \) and \( W_2 \)), in the proposed LNA design, the optimal value of \( W_1 \) and \( W_2 \) are 124µm and 48µm, respectively.

Simulation Results and Discussion

4. Simulation Results and Discussion

The proposed ultra-wideband LNA is designed and simulated by Advanced Design System (ADS) software using 0.18um RF CMOS process. Thanks to employing current-reuse and forward body biasing techniques, the proposed LNA’s supply voltage falls to 1.3V and consumes only 3.1mW power consumption. The simulated input reflection coefficient \( S_{11} \) is plotted is Fig.6, which shows that \( S_{11} \) is less than -13dB over 3GHz to 11GHz. Fig.7 shows the simulated output reflection coefficient \( S_{22} \), which presents that \( S_{22} \) is less than -14dB over 3-11GHz. The voltage gain (\( S_{21} \)) of the proposed LNA is plotted in Fig.8. From Fig.8, we can see that from 3GHz to 11GHz, the range of the voltage gain is from 16.8dB to 18.9dB. A result of shunt-series peaking technique, \( S_{21} \) has a great flatness and a higher voltage gain. The NF performance of the proposed LNA design is plotted in Fig.9, which shows that the range of NF is 1.9dB to 3.2dB over 3-11GHz. The input-third-order intercept point (IIP3) of the proposed LNA is plotted in Fig. 10, which features a simulated IIP3 of 10dBm. Fig.11 shows the layout of the proposed LNA, the total chip area is 0.87*0.81mm² including the input and output pads. Table II summaries performance of the proposed LNA and compares with previous works.

<p>| Table II Performance Summary and Comparison to Previously Reported LNAs |
|---|---|---|---|---|---|---|
| Reference | [3] | [4] | [8] | [17] | [20] | This work |
| Maximum gain (dB) | 10 | 8.6 | 15.3 | 14.8 | 11.7 | 18.2 |
| Minimum NF (dB) | 3.8 | 4.2 | 2.8 | 3.9 | 3.6 | 2.1 |
| BW (dB) | 2.7-9.1 | 0.03-6.2 | 2.5-11.7 | 2.4-11.2 | 1.5-8.1 | 3-11 |
| ( S_{11} ) (dB) | &lt;-10 | &lt;-16 | &lt;-10 | &lt;-12 | &lt;-9 | &lt;-13 |
| IIP3 (dBm) | - | +1.8 | - | -11.5 | 14.1 | 10 |</p>
<table>
<thead>
<tr>
<th>Area (mm²)</th>
<th>1.57</th>
<th>1.16</th>
<th>1.04</th>
<th>1.1</th>
<th>0.58</th>
<th>0.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_d$(mW)</td>
<td>7</td>
<td>9</td>
<td>11.6</td>
<td>3.4</td>
<td>2.62</td>
<td>3.1</td>
</tr>
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</table>

Fig. 5 Input reflection coefficient (S11)

Fig. 6 Output reflection coefficient (S22)
**Fig. 7** Power gain (S21) of the proposed LNA

**Fig. 8** NF of the proposed LNA

**Fig. 9** Input third order intercept point (IIP3) of the proposed LNA
5. Conclusion

This paper has presented the design of a highly linear, low power and high gain low noise amplifier for UWB receivers in 0.18um RF CMOS process. A common-gate (CG) topology amplifier with a low Q value was employed at the input stage for wideband input matching. In order to obtain a high power gain, a common-source (CS) topology amplifier with the shunt and series peaking technique was utilized in the second stage. The proposed LNA uses current-reuse and forward body biasing techniques to reduce power consumption. In addition, shunt-series peaking technique is employed to extend the bandwidth. Simulation results show that the proposed LNA achieves a minimum noise figure (NF) of 2.1dB, a 10dBm IIP3 with a maximum power gain of 18.2dB while consuming 3.1mW from a 1.3V supply voltage. Therefore, based on the simulated results, the proposed LNA is suitable as a building block in low power Radio Frequency (RF) front-end receiver for UWB systems.

Acknowledgements

The authors would like to thank the Open Fund Project of the research of platform for coal mine monitoring network based on wireless sensor networks in Department of education of Hunan Province No. 12C0986.
References


Also see:

- CMOS 3-11GHz UWB LNA employs current-reuse