Hierarchical test methodologies are being broadly adopted for large designs. They provide roughly an order of magnitude better ATPG (automatic test program generation) run time, reduce workstation memory requirements, and put the ATPG process much earlier in the design cycle than other methods. In hierarchical test, users need to add scan wrappers to blocks so the blocks can be treated as independent plug-and-play blocks with plug-and-play patterns.

Wrapper insertion is a change to the typical scan insertion practices, but it is fully automated with modern DFT tools so the effort isn’t very large. Often, most of the wrapper cells can simply reuse existing registered IO flops. The tools can automatically find the necessary cells for IO that aren’t registered or you can set a threshold for when to add a new dedicated wrapper cell. The rest of the process is pretty simple, but the clocking used for hierarchical test needs to support plug-and-play pattern retargeting. Thus, OCC (on-chip clock controller) design and location is a very important consideration with hierarchical test.

**Figure 1** is a logic diagram for an OCC provided in the Mentor AppNote MG580225. This app note describes the general design of the OCC from RTL (register transfer level) through ATPG and simulation. It is a flexible design for use with embedded test compression and hierarchical test. The same OCC structure is part of the automatic OCC insertion recently included in Mentor’s Tessent tool suite. The OCC ShiftReg is usually placed in part of a scan chain. ATPG tools determine the desired clock waveform and automatically determine the appropriate values to load into the ShiftReg to produce them. As a result, the programming of any number of OCCs is typically embedded in the scan data loaded with each pattern. No special programming or cycles are needed to set up these OCCs outside of the scan chain load data.

In the case of the hierarchical test methodology, it is easiest if the OCCs are all located within each
block. This way, all clock programming in ShiftReg is contained in each block-level scan pattern. Any set of block-level scan patterns with any type of clocking are completely plug-and-play and can be merged with any other block patterns at the top level of the design. OCCs in the blocks are the most flexible practice.

If it isn't possible to put OCCs within blocks, then hierarchical test and pattern retargeting to the top level design is still possible, but it is a little more complicated. The top-level OCC programming can't be embedded with the OCC ShiftReg loaded as part of the scan patterns because the scan patterns are created without the presence of the top-level design. Instead, the strategy is to set up the OCC to perform a repeated clock waveform for a group of patterns. The top-level OCC will not have the ShiftReg located with any scan chains, but as a test data register that can be statically loaded during test mode initialization. Then a set of block-level patterns with that same capture cycle clock waveform within each can be retargeted to the top level.

If you use a top-level OCC, the ATPG on each block will be a little less efficient than if each block has an OCC. The OCC clock waveforms need to be known during block-level ATPG. Block-level patterns are created in separate sets of patterns, one for each clock waveform. The Mentor tool's term for this type of restricted clock waveform is a "named capture procedure." When retargeting block-level patterns to the top level, the OCC is initialized for a clock waveform and then applicable patterns are retargeted to the top-level design. If multiple blocks share the same top-level OCC, then it is likely to result is less efficient pattern merging unless the two blocks happen to have the same number of patterns with that clock waveform.

On-chip clock controller design and location is an important consideration with hierarchical test. A programmable register based OCC at the block level provides the most flexibility and efficiency. Block-level patterns with block-level OCCs can be retargeted and merged with other block patterns at the top-level design independent of the clock waveforms.

Also see:
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