DDR4 memory interface: Solving PCB design challenges

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Introduction

DDR SDRAM technology has reached its 4th generation. The DDR4 SDRAM interface achieves a maximum data rate of 3.6Gbps per bit (i.e., clock rate of 1.8GHz).

There are four key challenges in designing the placement and routing of DDR4 SDRAM interface with multi-Gigabit transmission. The major challenges include the routing topology and termination scheme for nets with multiple receivers, routing technique to minimize crosstalk, method to mitigate the impedance discontinuity due to imperfect vias, and the method to maximize the timing margin of the data transmission.

These four challenges and the ways to overcome them are discussed in the subsequent section of this paper. The study is done by analyzing signal integrity using Mentor Graphics Hyperlynx with the import of IBIS models of Kintex UltraScale FPGA from Xilinx and DDR4 SDRAM from Micron.

Routing Technique for Multiple Receivers

With the growing size of data storage, more and more memory ICs are required to be accessed by the processor or memory controller. In the worst case condition, there could be as many as eight memory ICs (i.e., fan out) connected to the processor. The conventional way of routing (i.e., tree topology) creates the issue of trace stub which degrades the signal integrity of the transmission channel. The effect of trace stub is explained in (1), where resonant frequency or the bandwidth of the transmission line is inversely proportional to the stub length. In conventional tree topology, the trace stub is lengthened with the increase in number of receivers.

\[ f_o = \frac{c}{4 \times \text{stub\_length} \times \sqrt{D_k}} \]  

(1)

\( f_o \) = resonant frequency (Hz)

\( c \) = speed of light \((1.18 \times 10^{10} \text{ inches/sec})\)

\( \text{stub\_length} \) in inches

\( D_k \) = dielectric constant
The eye diagram analysis is conducted on an address signal net in tree topology with two SDRAMs driven by an FPGA at 2.4Gbps, shown in Figure 1. A 50 ohm resistor that serves as a parallel termination, is pulled up to 0.6V (i.e., half of the power rail) to amplify the dynamic range of the signal. The total trace length from FPGA to each SDRAM is 2 inch, where a stub length of 1 inch is seen by each SDRAM.

Referring to the specification of JEDEC and Micron, with bit rate of 2.4Gbps or unit interval (UI) of 416ps, setup time and hold time with respect to clock edge must be at least 62ps and 87ps respectively. The eye diagram at address pin of the memory is shown in Figure 2. The setup time is computed between the orange circle (i.e., when left half of eye opening crosses 700mV or logic 1 threshold) and the red vertical line (i.e., clock edge at the center of the eye opening). On the other hand, the hold time is computed between red vertical line and white circle (i.e., when right half of eye opening crosses 700mV or logic 1 threshold). This eye diagram indicates the setup time of 50ps, which violates the minimum timing requirement of the memory. This timing violation causes the issue of metastability where the receiver IC misinterprets the signal and results miscommunication between driver and receiver.

![Fig1. Simulation model of eye diagram for tree topology with 2 receivers](image1)

![Fig2. Eye diagram at memory with tree topology](image2)
The lower channel bandwidth due to trace stub attenuates the high frequency components that compose the rising and falling edges of the signal, and shrinks the eye opening at the memory. In order to overcome this problem, the conventional tree topology shall be replaced by the fly-by routing topology, shown in Figure 3. The first memory (i.e., U5) is connected to the driver (i.e., U4) with a 2 inch trace, while the second memory (i.e., U6) is cascaded to the first memory with a 1 inch trace. A parallel termination 50 ohm resistor is added at the end of the trace.

![Fig3. Simulation model of eye diagram for fly-by topology with 2 receivers](image)

The eye diagrams at memory U5 and U6 are illustrated in Figure 4A and Figure 4B respectively. The setup time and hold time in both figures are ~150ps respectively. The memory U6 does not experience stub effect at all with fly-by topology. A large eye opening is observed at memory U5 due to the fact that the long stub experienced by it, is terminated with a 50 ohm resistor. A properly terminated stub minimizes the reflection and attenuation of the signal.
The case study is further conducted with more receivers cascaded (i.e., 4 memory ICs in total) to the net, shown in Figure 5. The longest stub (i.e., 3 inch) is seen by the first memory, while shorter stub is experienced by the subsequent cascaded memory ICs. A parallel termination 50 ohm resistor is appended at the end of the channel (i.e., the last memory IC). The setup time and hold time of minimum 140ps at each receiver summarized in Table I, meet the timing requirement of JEDEC and Micron. By applying fly-by routing technique and properly terminating an opened long stub, attenuation of signal at the receiving end is alleviated.
Fig5. Simulation model of eye diagram for fly-by topology with 4 receivers

Table I. Summary of setup and hold time with fly-by topology

<table>
<thead>
<tr>
<th>Memory IC</th>
<th>Setup time (ps)</th>
<th>Hold time (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st</td>
<td>~150</td>
<td>~150</td>
</tr>
<tr>
<td>2nd</td>
<td>~150</td>
<td>~150</td>
</tr>
<tr>
<td>3rd</td>
<td>~145</td>
<td>~145</td>
</tr>
<tr>
<td>4th</td>
<td>~140</td>
<td>~140</td>
</tr>
</tbody>
</table>
Routing method to alleviate crosstalk

Routing Method to Alleviate Crosstalk

Crosstalk effect due to capacitive and inductive coupling from a signal to another becomes more severe at higher frequency and edge rate. At 2.4Gbps for DDR4 technology, the edge rate could be as high as 10V/\text{ns}. In order to minimize the coupling effect from the aggressor to the victim at high edge rate, the spacing between two adjacent signal traces shall be at least three times the trace width. However, the large trace spacing is tough to be implemented on the PCB with small dimension used in mobile computing device.

SDRAM applies source synchronous clocking scheme (i.e., non-interleaved routing), where all the signals in each single signaling group (e.g. address, data, control and command respectively) propagate in one direction simultaneously. In order to alleviate the crosstalk for traces with spacing of less than two times the copper width, the traces shall be laid out on inner PCB layer (i.e., stripline) instead of outer layer (i.e., microstrip).

In order to avoid misinformation at the receiver in the source synchronous clocking scheme, far end crosstalk (FEXT) must be minimal. In this section, the FEXT is studied by analyzing s-parameter and transient response at the receiver on stripline and microstrip with different trace length.

The simulation model of FEXT with coupled traces separated by one and a half times copper width is illustrated in Figure 6. Port 1 and 2 are the transmitting and receiving port respectively of the aggressor line. Meanwhile, Port 3 and 4 are the transmitting and receiving port respectively of the victim line. The plot of S-parameter (i.e., magnitude of \( S_{41} \) in dB versus frequency) that represents FEXT is shown in Figure 7. The \( S_{41} \) refers to the ratio of induced noise at the victim's receiver to the injected signal at the aggressor's transmitter. A more severe FEXT is indicated by the waveform with magnitude closer to 0dB. With reference to Figure 7, FEXT is minimal (i.e., less than -12dB) for coupled pairs on stripline compared to microstrip. The FEXT becomes more significant when the coupled length increases.

Fig6. Simulation model of s-parameter for FEXT
The FEXT is further studied by analyzing the transient response at the victim's receiver. The simulation model and result of transient response are shown in Figure 8 and 9 respectively. Referring to Figure 9, for 1 inch coupled length, the injected signal at aggressor (i.e., red curve) swings between 200mV and 1000mV. Meanwhile, the noise spurs with amplitude ~80mVpp (i.e., blue curve) and ~150mVpp (i.e., green curve) are induced at victim's receiver on stripline and microstrip respectively. The magnitude of noise induction with different coupled length on stripline and microstrip is summarized in Table II. The amplitude of noise induction increases with longer coupled pairs, and FEXT is much more severe on microstrip compared to stripline.
Table II. Summary of noise induction with different coupled length

<table>
<thead>
<tr>
<th>Coupled length (inch)</th>
<th>on Stripline (mVpp)</th>
<th>on Microstrip (mVpp)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>~80</td>
<td>~150</td>
</tr>
<tr>
<td>2</td>
<td>~110</td>
<td>~200</td>
</tr>
<tr>
<td>3</td>
<td>~120</td>
<td>~220</td>
</tr>
<tr>
<td>4</td>
<td>~190</td>
<td>~400</td>
</tr>
</tbody>
</table>

**Technique to Minimize Via Stub Effect**

The larger memory size of DDR4 SDRAM requires more bit width for data and address groups and increases the quantity of net to be laid out on PCB. Due to the limited space on PCB, different groups of signals are routed on different PCB layers. The transition of signal from one layer to another experiences a via stub effect. The bandwidth of the channel gets lower when the via stub becomes longer. The effect is explained in (2).

\[
f_o = \frac{c}{4 \times \text{via_stub_length} \times \sqrt{D_{ref}}} \tag{2}
\]

\(f_o\) = resonant frequency (Hz)

\(c\) = speed of light (1.18x1010 inches/sec)

\(\text{via_stub_length}\) in inches
$D_{\text{eff}} = \text{effective dielectric constant}$

The effect of via stub is analyzed with the simulation of insertion loss. With reference to the plot of insertion loss shown in Figure 10, the bandwidth decreases with the longer via stub. With via stub length of 120mil, 140mil and 160mil, the attenuation of signal is as much as -65dB minimum at 4.8GHz, 5.4GHz and 6.2GHz respectively. With much shorter via stub (i.e., less than 60mil), the insertion loss is lower than -5dB for frequency up to 9GHz. In order to keep the via stub short, if the driver and receiver ICs are placed on top layer of PCB, the traces shall be routed on layers closest to the bottom of PCB. Alternatively, micro via technique can be considered.

![Figure 10. Insertion loss plot for varying via stub length](image)

**Maximum Skew of Trace Length to Meet Timing Margin**

In order to be compliant with the specification of JEDEC, the maximum skew among all the signals shall be less than +/-2.5% of the clock period driven by the memory controller. All the signals of SDRAM are directly or indirectly referenced to the clock. For example, if the normal FR4 material with dielectric constant of 4 is used on PCB, at differential clock rate of 1.2GHz (i.e., 833ps clock period), the maximum skew shall be +/-125mil among all the signals. This number is computed with the equation of the propagation speed of signal on PCB, shown in (3).
\[ S = \frac{c}{\sqrt{D_k}} \]  \hspace{1cm} (3)

\( S \) = propagation speed of signal on PCB
\( c \) = speed of light (1.18x10^{10} \text{ inches/sec})
\( D_k \) = dielectric constant

**Conclusion**

DDR4 SDRAM operates at high data rate (i.e., from 1.6Gbps to 3.2Gbps) and the memory interface must be designed in a stringent way to comply with the specification set by JEDEC. All the major challenges discussed in this paper have to be overcome for excellent signal integrity to guarantee minimum bit error rate in the multi-Gigabit transmission.

**REFERENCES**


[2] DRAM Memory In High-Speed Digital Designs by Micron Technology


[8] LogiCORE IP UltraScale Architecture-Based FPGAs Memory Interface Solutions v4.2, Xilinx, 2013


Also see:

- [Addressing the challenges of transition to DDR4](#)
- [How to verify and debug next-generation memory](#)