IDDQ testing to improve yield and reliability, 1/2

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As technology shrinks, Yield and Reliability (YAR) are major challenges of SoC (System on Chip) production. There are many techniques available for increasing YAR. YAR of devices depend on testing strategies and the effectiveness of a testing methodology. (Design for Testing) DFT's main challenge is how to improve YAR; this paper describes the yield improvement by specifically using current testing. IDDQ testing (IDT) is a novel approach for testing faults which are left undetected by voltage testing. IDT is an essential quality testing requirement for today’s deep submicron devices (DSM) and Very deep submicron devices (VDSM).

Introduction

In order to achieve high quality VLSI chips, you must employ a rigorous testing strategy. Design for testing is one of the major challenges in VDSM technologies. There are many different testing techniques available such as Stuck-At (SA), Delay, functional, IDT and Burn-In testing.

This paper describes the merits of IDT for YAR improvement. Studies show that many defects in CMOS devices can be detected by IDT only. Most defects that cause logic or timing errors in a CMOS device can be also be detected via IDT. A good test strategy strongly depends on detection of non-targeted faults. The IDT method is based upon leakage current measurements during the steady state of a chip. Test effectiveness and quality is directly correlated with yield. Yields fall in to two types:

1. True yield (TY) = passed chips/total chips

Therefore, the main target is to increase the CVY rather than TY and to decrease the delta between TY and CVY. The main concern for testing is that customer quality chips (for the sake of brevity this will be abbreviated to GQC) will be passing as good chips but will be pooled in with chips that do not pass as GQC yet still pass a generic quality level. This decreases the reliability and homogeneity while decreasing CVY. Reliability is also as much important as yield, as reliability is essential for long life time of the chip.

Motivation

As technology moves towards VDSM and increasingly complex devices, the possibility of
manufacturing defects increases. There is a need to find a solution that increases testing quality and effectiveness. DFT, structural testing (ST), SA, Transition Delay Testing (TDT) and Path Delay Testing (PDT) are not reliable methods to detect defects like, Gate Oxide Shorts (GOS), SA Open (SAO), Bridging Faults (BF) in VDSM. Electrical current testing is becoming more important for VDSM devices, as current is affected by the faults like GOS, SAO, BF, etc. ST also increases the cost of testing. If we want fault coverage from 95 to 98% that requires a huge number of patterns for SA fault model which can be achieved by only current strobes. Through IDDQ, we can achieve 100% fault coverage using less current strobes. In CMOS, there are some defects which do not affect the functionality of the device, but will impact the device’s life time. Burn-In Testing (BIT) is method for calculating the life time of the device and it is also part of reliability testing however, BIT requires more test application time compared to other testing methods. With defects like GOS, SAO, BF, etc. that cannot be detected by ST, as these defects effect reliability and may have less impact on functionality, current testing is better solution.

**IDDQ Testing**

In current testing, we are not observing any output state at the PO (o/p) of SoC/design; we are measuring current at the power supply pins i.e. VDD or VSS. IDT can be done in two ways: using IDDQ fault model (IFM) and structural/functional patterns. EDA tools support both methods. IFM is used to generate patterns while using any EDA ATPG tool. If we want to use already generated structural/functional patterns, there are some selection criteria for structural/functional patterns. The selection criteria should be set up in such a way that by using less IDDQ strobes, we can get more test coverage.

Design requirements to make a chip IDDQ testable:

1) The device should be fully static CMOS design.

2) Separate power rails for
   i. I/O and core modules.
   ii. Analog and non-static CMOS modules.

3) Use IDDQ test mode signal to disable the transistors which is used to enable and disable the pull-ups and pull-downs.

4) Design doesn’t contain any unconnected modules and cell inputs.

IDT is more time consuming as it requires more time to stabilize the device. IDT is done at low frequency, thus consuming less power than SA, since SA requires a higher number of patterns. It has been reported that during testing, the occurrence of high switching activity increases high power dissipation and decreased the reliability of design.
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**Fig 1.** Test Strategies Comparison [3]

Experimental studies from SEMATECH as shown in Fig 1 shows that, IDT can detect more no physical defects than other testing methods. In this experiment, IDT is done with only few strobes. 1463 devices had defects can only be detected by IDDQ and these are defects that will not be detected by ST and functional testing. On the other hand, 36 devices pass the IDDQ but fail other testing methods.

**Yield Loss and Reliability Issues**

As we move to VDSM technology, the sources of yield loss (YL) are going to be increased. There are three types of YL, Catastrophic YL (CYL), Parametric YL (PYL) and Testing Related Yield Loss (TYL) [7]. CYL are functional failures such as, open/short circuits, which cause the part to not work at all. Extra or missing material particle defects are the primary causes of such failures. In PYL, the circuit functionality is working well, but it fails to meet some power and performance criteria, e.g. the device will work on a single VDD, but it may fail for entire range of VDD. Another example of sources of PYL is leakage for VDSM devices, intra-die or inter-die variations and temperature variations during circuit operation. PYL directly affect the reliability and life time of the device. Testing strategies cannot detect the all of the faults in a design. Due to limitations of the tester, higher probe resistance/impedance and lacking of test decision are the major source of TYL. It is highly desirable that these defects be detected during manufacturing test. The most common method, to screen these types of defects, is to burn-in the devices. Burn-in is an essential stress process by which devices are aged with proper excitation mechanisms. Burn-in patterns are mostly the functional patterns which target the limited area of the chip. Scan patterns are sometimes used but the selection criteria of scan patterns are so much tricky because the total number of scan patterns are larger than what may be applied into burn in boards.

In part 2, we will explore ways to improve yield and reliability with IDDQ Testing.

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