BIST schemes for ADCs

KUSHAL KAMAL Vandana Sapra - August 29, 2014

With an increasing number of complex circuits being integrated into SoCs, their testing requirements have become equally complex. While there are well established test strategies for digital circuits, the testing of analogue circuits is quite expensive and challenging. A commonly encountered analogue circuit is the analog to digital converter (ADC), and in this paper we will discuss the conventional method of testing ADCs, as well as the various built-in self-test schemes that can be used for their testing.

The traditional method of testing employs Automatic Test Equipment (ATE) feeding in arbitrary waveforms or test patterns to Device-Under-Test (DUT) and collecting test responses as seen in Figure 1. One popular and simplistic method to test an ADC is by a simple Ramp Test in which the ADC is configured to perform back to back conversions on a single channel. Then, a suitable ramp voltage is applied to the same channel so that all possible digital codes appear at the ADC output a fixed number of times. This output code is then compared against the expected ADC output. The difference between the expected and the actual output is calculated. The max. to min. variation of this difference is called TUE, or Total Unadjusted Error. On the test equipment, we program it to fail the part if the TUE is beyond an acceptable number. In Automotive MCUs, this figure can be up to ±2LSbs. Hence, if the ADC has a TUE of more than ±2LSbs, it is considered a bad part.

![Figure 1 Conventional test architecture](image)

The importance of ramp rate is evident from the above description. Let us see how an optimum ramp rate can be calculated, with the help of an example. Let us consider a 12 bit ADC that works at the rate of 1 Mega Samples Per Second (MSPS) for a Full-Scale range of 0-5V. The ADC gives 000(Hex) for input voltage of 0V and FFF (Hex) for 5V. The ADC output varies from 000 to FFF in 4096 steps as voltage rises from 0V to 5V. That means ADC output code changes by 1 when Input voltage increases by (5V-0V)/4096, that is, 1.22mV. If it is desired to get an output digital code to appear six times, we need to make sure that the ADC input does not increase by more than 1.22mV while ADC has made six conversions. With this understanding, the desired ramp rate can be calculated. The ADC gives one output code in 1μs. The input voltage must not change by more than 1.22mV in 6μs.
Thus the desired ramp rate is $1.22\text{mV/6µs}$ or $0.203\text{mV/µs}$.

There are multiple inherent disadvantages associated with this method:

- A lot of input and output data has to be stored and transferred from and to DUT.
- Effects of parasitic capacitances and external noise need to be taken into account.
- Measurement and evaluation of test responses takes considerable time, which directly adds onto production cost.
- For diagnostics and debug purposes, extra pins are required for tester that severely debilitates the parallel testing of different circuits.

A better option is to integrate self test hardware onto the chip. Systems equipped with self test hardware are capable of autonomous testing with no external stimulus generation and measurement requirement.

Built-in self test (BIST) schemes can also be categorized into offline and online. Offline BIST interrupts the normal operation and is not suited for real time environment, whereas online BIST runs in the background with no impact on normal operation. Online BIST requires redundant modules, so to implement this you would incur some cost. Online BIST can be further classified into concurrent and non-concurrent testing. In concurrent testing, normal functioning and testing can be done simultaneously, whereas in non-concurrent, testing is done in idle periods of the system.

The most simplified BIST test technique requires an on-chip waveform generator which generates an analog signal of higher resolution than the ADC, and records the number of times each unique digital code appears at the output. When choosing between various on-chip waveform generators, it has been found that using a triangular wave as input rather than a sinusoidal input has been advantageous. It saves memory required to save the output data\textsuperscript{[1]} and makes the calculations easy which in turn also saves the hardware operating resources. A histogram is created with the available data. The actual histogram is compared with that of an ideal one and various calculations are performed on the recorded data to compute Offset error, Gain error, Differential and Integral Non-Linearity error. A missing code is identified if corresponding count for any code is zero. For ramp input stimulus, the offset error is given by difference between the two extreme code histograms. Gain error is computed by comparing a number of non extreme codes’ histogram with their ideal values. DNL error is represented by the relative difference in actual and ideal ADC for each step size. INL is calculated by accumulating the sum of the DNL of all preceding codes.
The other popular BIST technique is DAC-ADC Loopback testing. It is beneficial to use this approach if both the converters are present on a chip. In this scheme, DAC is used to generate test signal for ADC (with this method also DAC must be of higher resolution than ADC, e.g., a 12 bit ADC won’t accurately test a 12 bit ADC, you need a 14 bit or 16 bit DAC). In this, a pseudo-random number generator or an up/down counter can be used to give input to the DAC, which gives its output to ADC via an analog input Mux shown in Figure 3. Since the expected digital output is known, it is compared against the input given to DAC. In loopback ADC testing, stimulus accuracy is crucial; the positive and negative slope rates must especially be equal, as any mismatch directly affects the ratio of code occurrences at either side of the code transition level.

The last BIST scheme to be discussed is Oscillation-based testing (OBT). It is an offline method. In this approach, the circuit under test is converted into an oscillator using some extra reconfiguration circuitry. The frequency of oscillation is compared with the reference value obtained from a good circuit to check if the circuit is faulty or good. In Oscillation Bist Testing of ADC, a test signal is made to oscillate between two transition voltages of the code width. As seen in Figure 4, the slope of test signal (a triangular waveform) is controlled by a logic circuit present in the feedback loop with ADC. Let’s take an example of a 2 bit ideal ADC with full scale voltage of 5V to understand more. For input voltage 0.5 LSB = 0.625V, output code transits from 00 to 01, so 0.625V is the transition voltage for code 01. Similarly the output code changes from 01 to 10 at 1.5LSB = 1.875V. Now the difference of transition voltages of two consecutive codes gives us the code width or step size. Hence DNL can be calculated for any code as it is given by difference in actual step size and ideal step size. Similarly other static performance parameters of the ADCs can be calculated. The slope of the triangle wave signal is inverted by one sample time after the sampled input signal attains or crosses the threshold voltage. The measured frequency of the triangle wave signal would indicate if the circuit is good or bad.
On-chip built in self-test (BIST) has many advantages over conventional test schemes:

- Since it is completely an on-chip solution, it can be used during production testing as well as field testing. It saves a lot of test time and cost. The time that goes into setting up complicated tester requirements and designing probe cards gets saved. Reduced test time directly reduces time-to-market.
- As every component is self contained, there is no influence of external noise, hence the results are more accurate and reliable.
- Traditional off chip methods involving high speed testing require expensive Automatic Test Equipment (ATE), which can cost tens of millions of dollars.
- Whereas in conventional chip testing, if a die is pad limited, it makes parallel testing of ADCs challenging due to limited I/Os available for forcing input signals and observing results, BIST schemes has no such issues of controllability and observability.
- For devices used in safety-critical applications, BIST hardware is very important to check the functionality at regular intervals, when just production testing is not enough.

REFERENCES:

1. Implementation of a Linear Histogram BIST for ADCs; F. Azaïs, S. Bernard, Y. Bertrand, M. Renovell
2. Built-in Performance Characterization of Embedded Mixed-signal Circuits; Hongjoong Shin

Also see:

- MBIST verification: Best practices & challenges
- Challenges in LBIST validation for high reliability SoCs
- Adding CRC to BIST improves SoC safety & reliability
- Redundancy for safety-compliant automotive & other devices