Signal integrity and power integrity in high-speed design

Patrick Carrier - August 26, 2014

Editor's Note: Signal integrity (SI) and power integrity (PI) are two critical topics in high-speed design and a major focus at DesignCon. I asked Mentor Graphics’ Pat Carrier to provide some perspective on their unique challenges, particularly in terms of simulation.

Signal integrity (SI) and power integrity (PI) are two distinct but related realms of analysis concerned with proper operation of digital circuits. In signal integrity, the main concern is making sure that transmitted 1s look like 1s at the receiver (and same for the 0s). In power integrity, the main concern is making sure that the drivers and receivers are provided with adequate current to send and receive 1s and 0s. So, power integrity could be considered a subset of signal integrity. Really, they are both analyses concerned with the proper analog operation of digital circuits.

The Necessities for Analysis?

If computing resources were infinite, these different types of analysis might not exist. Entire circuits would be analyzed at once, and problems in one part of the circuit would be identified and eliminated. But other than being bound by the reality of what can practically be simulated, the advantage of having different realms of analysis is that specific problems can be addressed in groups without falling under the category of “anything that could possibly go wrong.”

In signal integrity, for instance, the focus is the link from transmitter to receiver. Models can be created for just the transmitter and receiver, and everything in between. This makes simulating signal integrity fairly straightforward. Power integrity, on the other hand, can be a little more difficult to simulate, since the “boundaries” are a little less defined, and really have some dependence on items in the signal integrity realm.

In signal integrity, the goal is to eliminate problems with signal quality, crosstalk, and timing. The same types of models are needed for all these types of analysis. These include models for the drivers and receivers, the chip package, and the board interconnect, which consists of traces and also vias, discretes, and/or connectors. The driver and receiver models include information about the buffer impedance, edge rate, and voltage swing. Often, IBIS or SPICE models are used as the buffer models. These models are used with the interconnect models to run simulations to determine what the signal will look like at the receiver.

The interconnect will consist mainly of circuit board traces, which behave like transmission lines. Such transmission lines, or T-lines, have characteristic impedances, delays, and loss. Their characteristics determine how the connected drivers and receivers interact with one another. The electromagnetic properties of the interconnect must be solved using some type of field solver, which characterizes them in terms of a circuit element or S-parameter model that can be used with a signal integrity simulator. Most traces can be modeled as a uniform 2-dimensional cross-section. That
cross-section is sufficient to calculate the characteristic impedance of the trace. It is that impedance that will affect the shape of the waveform at the receiver on a signal line. The most basic of signal integrity analysis involves setting up a board stackup, including appropriate dielectric layer thicknesses, and finding the right trace width to achieve a certain target impedance for the traces.

Traces are relatively easy to model compared to vias. Proper via modeling becomes important when doing signal integrity analysis on faster signals. Signals in the multi-GHz range often require a model from a 3D field solver to be appropriately characterized. Fortunately, these signals tend to be differential, which keeps their effects relatively localized. Fast, single-ended signals that pass through vias interact very strongly with the power distribution network (PDN). The return currents from these vias pass through nearby stitching vias, stitching capacitors, and/or plane pairs, the same components that make up a PDN and need to be modeled for power integrity analysis.

In power integrity analysis, higher-frequency energy is distributed through transmission planes. This immediately makes the analysis more complex than basic signal integrity, since energy is moving in x and y directions, as opposed to just one direction down the transmission line.

At DC, modeling is relatively simple in that the series resistance of traces, plane shapes, and vias needs to be calculated. But for high frequencies, analyzing the impedance between power and ground at various locations on the PDN requires complex calculations. The impedance will vary based on board location - where the capacitors are placed, how they are mounted, and what type and value of capacitor they are.

High-frequency behavior, such as mounted inductance and plane spreading inductance, need to be included in the modeling in order to generate accurate results for decoupling analysis. There is a simple version of decoupling analysis usually referred to as lumped analysis, where the impedance of the PDN is calculated as if it were one node. This is usually a good, quick first-pass type analysis to ensure that there are enough capacitors and that they are the right values. Then, running a distributed decoupling analysis ensures that all the impedance needs of the PDN are met at various locations on the board.

**Signal Integrity Simulations**

Signal integrity simulations focus on three main issues of high-speed signaling: signal quality, crosstalk, and timing. For signal quality, the goal is to get signals with nice clean edges, no excessive overshoot, nor ringback. Usually these problems can be solved by adding some type of termination to match the impedances of the driver to the transmission lines. For multi-drop busses, matched impedances aren’t always possible, so a combination of termination and length changes on the topology are necessary to control reflections such that they do not adversely affect signal quality and timing.
Figure 2. Using signal integrity analysis and design space exploration to eliminate signal quality and crosstalk issues.

These same simulations can be run to determine the flight times of the signals as they travel through the board. Board timing is an important part of the system timing, and gets affected by the lengths of the lines, their propagation speed as they travel through the board, and the shape of the waveform at the receiver. Since the shape of the waveform determines when the received signal crosses the logic threshold, it is essential to the timing. These simulations usually drive changes in the length constraints put on the traces.

Another signal integrity simulation that is usually run is crosstalk. This involves multiple transmission lines coupled to one another. As traces get packed into dense board designs, knowing how much energy they are coupling onto one another is essential to eliminating errors due to crosstalk. These simulations will drive minimum spacing requirements between the traces. **Power Integrity Simulations**

In power integrity analysis, the main types of simulations are DC Drop analysis, decoupling analysis, and noise analysis. DC Drop analysis involves the analysis of complex trace and plane shapes on the PCB to determine how much voltage is being lost due to the resistance of the copper. Also, areas of high current density can be identified using DC Drop analysis. These can actually be co-simulated with a thermal simulator to see the heating effects. Fortunately, the solution to DC Drop problems is simple: add more metal. This additional metal may take the form of wider and/or thicker trace and plane shapes, additional planes, or additional vias.
Decoupling analysis, which was discussed briefly above, is aimed at determining and minimizing the impedance between power and ground at various IC locations on the board. Decoupling analysis usually drives changes in the value, type of, and number of capacitors used in the PDN. As such, it requires models of the capacitors that include their parasitic inductances and resistances. It can also drive changes to how the capacitors are mounted and/or changes to the board stackup in order to meet the low impedance requirements.

Types of noise analysis can vary. They can include noise from the IC power pins propagating around the board and be controlled by the decoupling capacitors. It can be an investigation of how noise is coupling from one via to another. It can be an analysis of simultaneous switching noise. In many cases this noise is caused by signals switching, from 1 to 0 and 0 to 1, so it is closely related to signal integrity. In all cases, however, the ultimate goal of these power integrity analyses is to drive changes to the PDN: power/ground plane pairs, traces, capacitors, and vias.

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An Integrity Cocktail?
The PDN will not only act as a means of delivering current to ICs, but also as a return current path
for signals. A great deal of the crossover between signal and power integrity occurs at vias. For a single-ended signal passing through a via, it is the PDN that acts as the return current path for that signal. Nearby vias or capacitors provide a path for the return current to move from one plane to the next. So, the PDN actually determines the impedance and delay characteristics of that single-ended via, and is crucial for accurate modeling of faster single-ended signals like DDR3 and DDR4. Using that same SI/PI combined via model, coupling from one via to the next can be analyzed, as well as coupling from signals into the PDN through vias.

Similarly, the PDN is crucial to minimizing the noise that can be caused by multiple signals switching together, commonly referred to as SSN (simultaneous switching noise). If the PDN impedance is too high at the power pins of an IC, when all the drivers switch at once, their switching current will induce a voltage that can be seen on the signals themselves.

This problem can be eliminated by utilizing decoupling analysis to design a nice low-impedance PDN. Simulating this problem in its entirety to see the effect on the signals requires the capability to perform both signal integrity and power integrity analysis together. SPICE models for the drivers have traditionally been used to perform this kind of analysis, but newer IBIS models also have the appropriate infrastructure to include the effects of the PDN in looking at signal integrity.

The analysis of both signal integrity and power integrity is vital to a successful high-speed digital design. They provide valuable insight into what design changes need to be made. And as modeling methods and computing capability improves, being able to simulate both flavors of integrity together will allow a clear understanding of how circuits actually behave, what kind of margins truly exist in a design, and how they can achieve the best possible performance.

**Further Reading/References:**

1. Fundamentals of Signal Integrity Analysis
2. Power Integrity Effects of HDI
3. Design of Power-Distribution Networks in the Era of Proliferating Voltage Levels and High Current Demands

**Also See:**

- Measure PDN on a budget
- PDN issues occur in the simplest circuits
- Perform signal integrity testing without a scope