Digital transmission of analog signals through a long distance I2C bus

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The Inter-Integrated Circuit Bus (I2C) is a synchronous serial data communication bus in which the master initiates the communication and the slaves are controlled by addressing. In the I2C bus, nodes are easily incorporated because there are only two signals to be connected (SDA for data and SCL for clock), which are open-drain lines. Therefore, it is expected that the capacitance in these lines is the main cause of limiting the transmission rate and distance between nodes [1]. To be extended, the use of buffers, with capability to identify the data direction, is necessary. In this design, the benefits of the PCA9605 IC are exploited.

The PCA9605 is a monolithic CMOS integrated circuit for bus buffering in applications including I2C-bus. The buffer extends the bus load limit by buffering both the SCL and SDA lines, allowing the maximum permissible bus capacitance on both sides of the buffer. In its most basic implementation, the buffer will allow an extended number of slave devices to be attached to one master device. In this design, the master is a PIC microcontroller [2] and the slaves are two data converters, one analog-to-digital and other digital-to-analog. The PCA9605 direction pin (DIR) is fixed to ground since the clock is provided by the master (unidirectional clock mode). The general schematic is depicted in Figure 1.

The current data is firstly acquired from the generator by U2 ADC. Then, it is transmitted by the buffer U3 through the cable and repeated by U4. Therefore, the SDA data line needs to be driven in both directions, from U3 to U4 and vice-versa. Finally, the digitized signal is generated by the U5 DAC. If the cable is longer, the circuit can be extended by inserting another buffer in the middle of it. In this way, hundreds of meters of wired distance can be covered [3].

Figure 1. Circuit interconnecting two nodes in an extended I2C bus.

Figure 2 shows the transmission of the DAC address (0xC0) through the cable bus at 125 kHz. The Channel 1, which corresponds with the bus side SDA wire (U4, pin 6), is conditioned by the buffer that eliminates the spikes and capacitive interferences from the clock wire, as well as RC effects due
to the open collector working with the pull-up resistor and the wire's capacitance. The Channel 2 shows the conditioned SDA data signal (U4, pin 7) and the Channel 4 (U4, pin 2) the clock SCL after being conditioning. The clock signal in the cable (U4, pin 3) is shown in Channel 3, and in Channel 4 it is shown after being conditioned (U4, pin 2).

If the system is tested by sending a unipolar analog signal with the voltage amplitude of the full input range in the ADC U2, the waveform depicted in Figure 3 is obtained in the output load of the DAC U5. This design exploits the characteristics of the ADC and DAC circuits that allow them to work with rail-to-rail signals. This performance at low frequencies can be improved by adding a low pass filter in the DAC output in order to reduce the sampling and reconstruction noise.

Figure 2. Signals in the slave node before and after the buffer.

Figure 3. Full scale input sinusoidal signal transmitted through the I2C.

References