Understanding layers in the JESD204B specification: A high speed ADC perspective, Part 1

Jonathan Harris, product applications engineer, Analog Devices, High-speed converter group - September 24, 2014

Editor’s note: In this two-part article, the author will help designers understand how high speed ADCs can properly use and understand how to use to your design advantage the JESD204B standard for the ADC to FPGA interface. Part 1 will discuss an Introduction and Data Flow through the layers of the JESD204B interface, as well as the Application and Transport layers discussed in depth. Part 2 will continue with a thorough discussion of Data Link layer as well as the Physical Link layers.

Introduction

As high speed analog-to-digital converters (ADCs) move into the gigasample-per-second (GSPS) range, the interface of choice for data transfer to FPGAs (or custom ASICs) employs the JESD204B protocol. In order to capture RF spectrum higher in the frequency range, wideband RF ADCs are necessary. With this push to GSPS ADCs that capture wider bandwidths and allow for more configurable SDR (software defined radio) platforms, a high speed serial interface, JESD204B in this case, is necessary. It is important to understand that the JESD204B standard is a layered specification.

Each layer within the specification has its own function to perform. The application layer allows for configuration and data mapping of the JESD204B link. The transport layer maps conversion samples to and from framed non-scrambled octets. The scrambling layers can optionally take those octets and scramble or descramble them in order to reduce EMI effects by spreading the spectral peaks. Scrambling would be done in the transmitter and descrambling done in the receiver. The data link layer is where the optionally scrambled octets are encoded to 10-bit characters. This layer is also where control character generation or detection is done for lane alignment monitoring and maintenance. The physical layer is the serializer/deserializer or (SERDES) layer responsible for transmitting or receiving the characters at line rate speeds. This layer includes the serializer, the drivers, the receivers, the clock and data recovery, etc. The figure 1 shows the arrangement of these layers within the JESD204B specification. To better understand the specification a closer
examination of each layer is beneficial so that it can be seen how the ADC samples are mapped to 8b/10b serialized words.

**Figure 1. Simplified Data Flow Through JESD204B Layers**

**Application Layer**

The application layer allows for special user configurations and for sample data to be mapped outside of the typical JESD204B specification. This can allow for a more efficient use of the interface to accomplish power reductions and other benefits. The transmitter (ADC) and receiver (FPGA) must both be configured for these special configurations. This is important to remember. The receiver and transmitter must be configured identically so that data is transmitted and interpreted correctly. Configuring the application layer in a unique way can be beneficial for ADCs that need to pass data in sample sizes that may be different than the N’ (the number of transmitted bits per sample). This could allow for multiple samples to be repacked in such a way that the lane rate can be reduced and the overall link efficiency increased.

**Transport Layer**

Next, take a closer examination of the transport layer of the JESD204B specification. The transport layer takes the ADC samples and adds information (or padding) to generate nibble groups (usually on 4-bit boundaries). This information is in the form of tail bits or control bits which can provide additional information about the transmitted data. The transport layer arranges these nibble groups into frames. It is important to note that the transport layer delivers the samples to the data link layer as parallel data. The width of the parallel data bus is determined by the framer architectures (single byte is 8 bits, dual byte is 16 bits, etc.) The serializer has not yet been reached in the data flow at this point.
A single ADC can be mapped to a single-lane link or can be mapped to a multi-lane link. This configurability is especially handy for GSPS ADCs used in wideband RF applications where the sample rate dictates that multiple lanes be used in order to meet limits on lane rates. Multiple converters can also be mapped onto multiple lanes for \( M \) number of ADCs in the same device. The ADCs can be mapped to a single-lane link or into a multi-lane link consisting of \( L \) number of lanes. In some cases an ADC may need multiple lanes. The lane rate maximum of a given ADC determines this. For example, the 12-bit 2.5 GSPS AD9625 has a lane rate maximum of 6.5 Gbps. This means that with \( N' \) equal to 16, a total of 8 lanes are required.

Sometimes the lane rate may be limited by the FPGA in the system. For customers using GSPS ADCs in their RF applications, one design parameter may be cost. In order to drive the cost down, an FPGA with lower lane rate capability may be used. For example, the 14-bit 1.0 GSPS dual channel AD9680 has a maximum lane rate of 12.5 Gbps. The AD9680 has four output lanes and can be configured to use decimation to lower the sample rate and thus the lane rate. This is serving two purposes, a lane rate reduction and a bandwidth selection for a specific RF application.

### Back to JESD204B parameters

Now, moving back to the JESD204B parameters, the \( N' \) parameter gives the JESD204B word size. The converter sample resolution is broken down into four-bit nibbles. A 14-bit converter, as well as a 16-bit converter, has four nibbles, while a 12-bit converter has three nibbles. If \( N' \) is set to 12 for the AD9625, the number of required lanes can be reduced by 2 such that 6 lanes are required to maintain a lane rate of less than 6.5 Gbps. The conversion samples (\( S \)) are recommended to be mapped into JESD204B words on 4-bit nibble boundaries. Figure 2 shows the mapping of ADC samples into the serial lanes. It is parameterized such that it covers the many potential cases that can be realized with JESD204B.

The \( N' \) parameter is found by multiplying the number of nibbles by four. It can be advantageous to both the transmitter and receiver to set \( N' \) to 16 for converters with resolutions ranging from eight bits to 16 bits. This allows for the same transmitter and receiver to be used for multiple converters, easing overall system design. A non-complete nibble has room for either control bits (\( CS \)) or tail bits (shown as \( TT \) below in Figure 2) as defined by the JESD204B standard. The equation \( N' = N + CS + T \) must be satisfied. Control bits, if any, are appended after the LSB to each conversion sample.

After using the number of converters, the number of samples per frame, the JESD204B word size, and the maximum lane rate to calculate the number of lanes, we can determine the number of octets transmitted per frame, \( F \). In order to determine this parameter, the following equation can be used: 
\[
F = \frac{M \times S \times N'}{(8 \times L)}
\]. For more on JESD204 link parameters refer to reference 1 which describes the link parameters in greater detail. In addition, there is a four part webinar series that provides further information on the JESD204 standard beginning with the transport layer.
The transport layer determines how to pack the data from the ADC based on the link configuration parameters that have been defined for a given device. These parameters are transmitted from the ADC to the FPGA during the Initial Lane Alignment Sequence (ILAS). These settings are configured via a Serial Port Interface (SPI) that would set register values on the ADC and the FPGA to define the link configuration parameters. A checksum is generated from the parameters and transmitted so that the receiver (FPGA) can verify the link configuration parameters were received correctly.

The parameters sent across the link are not used to configure the receiver; they are only used to verify that the link parameters match. If an error is detected, the FPGA will report this error via an interrupt which is defined in the error reporting of the JESD204B specification. For more on the link configuration parameters, please see more in reference (1) at the end of this article.

Please stay tuned to Part 2 which will be posted shortly on EDN.

References


(4) JESD204B Serial Interface for Data Converters, July 2011.

(5) System Interface Level 5: Common Electrical Characteristics for 2.488-3.125 Gbps Parallel Interfaces - OIF-SxI5-01.0, October 2002.


More articles on this topic

The JESD204B interface collection of articles on EDN: Board footprint saver and speed enhancer