The size of designs continues to grow and IC manufacturers are pushing for higher test quality, especially in mission-critical applications such as transportation and medicine. More advanced nodes also require new types of tests to catch more subtle defects. The result: exploding test pattern set sizes that result in longer test times and the need for more tester capacity for a given device ship rate. That drives up manufacturing cost.

To help manage the size of test patterns without sacrificing test quality, DFT (design for test) software tools employ compression techniques to reduce the size of the patterns that have to be transferred to the device under test (DUT). The technique involves adding a small amount of circuitry to the DUT and special processing of the test patterns when they are generated by the ATPG (automatic test pattern generation) software. Test compression levels of two orders of magnitude compared to uncompressed patterns are routinely achieved. Once compressed test patterns are expanded within the device under test, they can be applied to a much higher number of shorter internal scan chains than is possible for patterns applied externally. Thus, compression also results in reduced test times.

**Figure 1** shows a basic block-level implementation of the on-chip compression scheme and how it connects to the tester. The core design and its scan chains (see part 1 of this series) are in the middle of the upper block. The additional on-chip logic includes a decompressor on the input side, which expands the compressed patterns and loads them into the scan chains within the DUT. A compactor on the output side captures and compresses the test results and returns the data to the tester for comparison against expected results. This logic is only active in the scan path during test and doesn't affect the IC’s functional design or performance.
Figure 1. Example of on-chip test compression logic.

Unknown States

For most scan test pattern results, some number of Xs, or unknown values, are captured in the scan cells. These Xs come from many sources such as uninitialized flip-flops and memories. If not handled properly, these Xs cause big problems because they can mask the captured response values that need to be observed for each test pattern. This problem leads to a decrease in test coverage and test compression levels. In the general case, designers need to modify the design to eliminate the sources of Xs. Advanced test compression solutions, however, have methods to block these Xs by using scan-chain masking techniques. So high test coverage and compression levels can still be obtained.

Low-pin-count testing

As device complexity increases and fabrication-process defects change, DFT is trending toward more tests to maintain quality. Traditional scan testing uses connections between the tester and functional I/O pins on the DUT to transfer the test pattern data and to return captured responses to the tester. For many advanced chips, however, the number of digital pins that can be made available for test
channels may be small compared to the complexity of the chip. In these cases, engineers can create a minimal test interface to the DUT using a technique called RCPT (reduced pin count test). RPCT enables multi-site testing, where the available tester channels are used to test two or more chips in parallel, increasing test throughput. Another common motivation for RPCT is to relieve top-level routing congestion in modular designs by applying high quality test to each IC block using as few as one or two channels.

RPCT provides control and observation access that's close to the I/O pins but without direct tester contact (Figure 2). The idea is to reuse scan cells located at functional I/O pins (so-called boundary-scan cells) for control and observation during scan testing.

Figure 2. RPCT techniques indirectly control and observe functional I/O through boundary-scan cells so that tester contact is not necessary (CUT=circuit under test).

These boundary-scan cells are controlled through a boundary scan state machine and a four-pin-o-five-pin TAP (test access port). The TAP is set up so that after initialization, each boundary-scan cell behaves as if it were a normal scan cell. The TAP remains in a static state after being initialized. Thus, ATPG has access close to the functional I/O pins during normal scan test pattern generation. This means that external connection to the other (functional) pins is not necessary during scan test. Even at-speed scan testing can be performed efficiently by using RPCT techniques, where the boundary scan cells stay in shift mode during the at-speed launch cycle to avoid launching X states from the unconnected functional I/O.

Using these techniques with aggressive test compression can enable effective testing with only one or two test channels, and without loss of test coverage or test quality. In practice, a test setup nominally using 40 tester channels can be reduced to just two channels while still running test patterns 20 times faster than the non-compression baseline. Importantly, the ability to perform scan diagnosis can be preserved so that diagnosis resolution is similar to non-compression scan diagnosis results.

Next time I’ll discuss some new test techniques that can improve the quality of test, especially for
advanced node ICs employing FinFET transistors.

Also See
- Design for test boot camp, part 1: Scan test
- Hierarchical test improves pattern application efficiency
- Improve test quality and reduce DFT costs
- Contactless Testing
- Address FinFET test challenges
- Test compression