The purpose of a **PLL** is to generate a frequency and phase-locked output oscillation signal.

To achieve this goal, prior art essentially functioned by frequently changing the **PLL** output frequency according to the phase error (i.e. the **faster/slower** phase relationship) to generate a momentary, but not static, frequency and phase locked output oscillation signal. This frequent back-and-forth change in **VCO** frequency creates significant **jitter** and a longer **settling time** because when phase is correct (locked), frequency is likely wrong (unlocked), or when frequency is correct (locked), phase is likely wrong (unlocked).

### 1. Field of the Invention

The present invention relates to Phase Locked Loops (PLL) including **PLL** using Voltage Controlled Oscillators (VCO) and Digital Controlled Oscillators (DCO).

### 2. Description of Prior Art

Analog **PLL** are generally built with a phase detector, a low pass filter, a VCO and a frequency divider in a negative feedback configuration.

Digital **PLL** are generally built with a time-to-digital converter, a digital loop filter, a DCO and a frequency divider in a negative feedback configuration.

A **VCO** or **DCO** efficiently provides oscillation waveform with variable frequency. **PLL** synchronises **VCO** / **DCO** frequency to input reference frequency feedback.
VCO output frequency $F_{vco} = K_{vco} \times V_{ctl}$, where $K_{vco}$ is constant gain over most of the usable control voltage range, and $V_{ctl}$ is VCO control voltage.

An important part of a PLL is the phase detector or time-to-digital converter. This compares the phase of the two inputs to the detector and produces a corrective voltage signal to control the oscillator so that the phase between the inputs becomes zero. The two inputs of the phase detector are usually the reference and the divided output of VCO or DCO.

The purpose of PLL is to generate a frequency and phase locked output oscillation signal.

However, prior art cannot achieve the desired purpose because (1) VCO and DCO are frequency variable and controllable, they are not phase variable and controllable and (2), using phase error to correct frequency is improper because it is a conflict control and leads to infinite jitter in PLL output (i.e. deviation of VCO/DCO output edges from their ideal placement in time). Due to these two reasons, neither frequency nor phase will actually be locked – making PLL performance difficult to improve.

Prior art essentially functioned by frequently changing the PLL output frequency according to the phase error (i.e. the faster/slower phase relationship) to generate a momentary, but not static, frequency and phase locked output oscillation signal. This frequent back-and-forth change in VCO frequency creates significant Jitter and a longer settling time because when phase is correct (locked), frequency is likely wrong (unlocked), or when frequency is correct (locked), phase is likely wrong (unlocked).

3. Summary of the Invention

An ideal PLL should generate a very stable output oscillation signal with a truly locked frequency, and a truly locked phase (i.e. both frequency and phase should not change with time).

Two signals can be truly phase locked (phase will not change with time) only if their frequencies are the same or locked (within a narrow, allowable range) first.

This can be more clearly explained by following mathematical equations.

Let $\Delta \Phi (t) =$ relative phase error, $\omega_1 =$ frequency1, $\omega_2 =$ frequency2, $(\omega_1 - \omega_2) =$ frequency error, $\theta_1$
is \( \omega_1 \)'s initial phase (constant), \( \theta_2 \) is \( \omega_2 \)'s initial phase (constant), and \( t = \text{time} \),

\[
\text{Ref}(t) = M \times \sin (\omega_1 t + \theta_1) = M \times \sin (\Delta \theta_1(t) + \theta_1), \quad (1-1)
\]

\[
\text{Div}(t) = N \times \sin (\omega_2 t + \theta_2) = N \times \sin (\Delta \theta_2(t) + \theta_2), \quad (1-2)
\]

\[
\Delta \Phi(t) = (\omega_1 - \omega_2) t + (\theta_1 - \theta_2) = (\Delta \theta_1(t) - \Delta \theta_2(t)) + (\theta_1 - \theta_2), \quad (1-3)
\]

According to equation (1-3), at any time, when \( \omega_1 = \omega_2 \) or \( (\omega_1 - \omega_2) = 0 \), \( \Delta \Phi(t) = \theta_1 - \theta_2 \) becomes a constant, the two signals will have a fixed phase relationship and, therefore, no Jitter, otherwise, relative phase error \( \Delta \Phi(t) \) will change with \( t, \omega_1 \) or \( \omega_2 \) - meaning that the distance between \( \text{Ref}(t) \)'s and \( \text{Div}(t) \)'s rising or falling edges will change with time and therefore, Jitter will happen.

Prior Art (faster/slower feedback control) can be expressed by the following advanced mathematical equation.

\[
\Delta \Phi(t) = \int \Delta \omega(t) dt = \int (\omega_1(t) - \omega_2(t)) dt
\]

when phase is locked, mathematically, \( \Delta \Phi(t) \approx \text{constant} \) (even \( \omega_1(t) - \omega_2(t) \neq 0 \), the integral result \( \Delta \Phi(t) \) is still possible to be a constant). But in reality, \( \Delta \Phi(t) \) will change (within a narrow, allowable range) with \( t, \omega_1(t) \) or \( \omega_2(t) \). That is why Jitter will be inevitable.

The present invention provides a new, and different approach by (1) replacing prior single loop PLL with a frequency-locked loop and a phase-locked loop so that the frequency loop is controlled by frequency error and the phase locked loop is controlled by dynamic phase error ( the difference between the first static phase error and each consecutive static phase error ) instead of static phase error. The control target of the frequency locked loop is a frequency variable unit / device like VCO and DCO. The control target of the phase locked loop is a phase delay variable unit / device. (2) providing a simple, high-resolution frequency error detector and an improved proportional and integral feedback control scheme for the said frequency locked loop. (3) providing a dynamic phase error detection and correction for the said phase locked loop.

With the present invention, several advantages are obtained, (1) frequency and phase can be separately controlled and truly locked (theoretically, error to zero), resulting in significant reduction of Jitter (eliminate using phase error to control VCO or DCO). (2) fast output response with limited or no overshoot / undershoot in frequency while ensuring high frequency accuracy when frequency
is locked. (3) simple in design and easy for manufacturing.

4. Brief Description of the Drawings

4. Brief Description of the Drawings

FIG 1 provides an embodiment of block diagram for the frequency and phase locked loops according to the present invention.

FIG 2 provides an embodiment of block diagram for the frequency locked loop according to the present invention.

FIG 3 provides an embodiment of block diagram for the phase locked loop according to the present invention.

FIG 4 shows signal waveform relation according to the present invention.

FIG 5 is a block diagram of the prior art Analog / Digital PLL.

FIG 6 is a graph of VCO gain.

FIG 7 is a graph of output Jitter of prior art Analog / Digital PLL.

5 Description of Preferred Embodiment

In FIG 1, a frequency locked loop is built of Frequency Detect, Logic 1, D/A1, D/A2, VCO/DCO, Phase Control, Divider A, Divider B and Divider C.
FIG 1 provides an embodiment of block diagram for the frequency and phase locked loops according to the present invention.

A phase locked loop is built of **Phase Detect, Logic 2, Phase Control, Divider A, Divider B** and **Divider C**.

A frequency and phase locked loop is built of connecting the output of the frequency locked loop $Out'(t)$ with the input of the phase locked loop to output a frequency and phase locked signal $Out(t)$.

In the frequency locked loop, $Out(t)$ is first divided by **Divider A** to generate a signal **CLK**. **CLK** is provided to **Divider B** for further dividing and to **Frequency Detect** as high speed sampling clock for $Ref(t)$ and $Div(t)$. The output of **Divider B** generates a signal **Slope**. **Slope** is provided to the **Logic, D/A1, D/A2** as a clock of a counter used for frequency coarse tune and to **Divider C** for further dividing. Because the frequency of signal **Slope** will determine the rising speed of the counter’s outputs which are converted to a frequency control voltage by **D/A1** for frequency proportional / coarse control, it is named **Slope**.

Changing **Divider B** can change the slope of proportional frequency control. **Divider C** generates signal **Div(t)**. **Div(t)** is provided to **Frequency Detect** where its frequency is compared with and subtracted by reference signal **Ref(t)**. **Frequency Detect** generates a frequency error signal **Er1** and an enable signal **EN2**. **Er1** is the frequency difference / error between **Ref(t)** and **Div(t)** and is provided to **Logic1, D/A1, D/A2** for setting the **D/A1**’s output at the end of proportional control (coarse tune) and for **D/A2**’s integral control (fine tune) so that **Er1** will be or approximate to zero and frequency can be locked. **EN2** is an enable signal which will become ‘1’ when frequency is locked and is provided to **Phase Detect** to enable phase error detect.

The output of **Logic1, D/A1, D/A2** block is provided to control **VCO/DCO**. The output of **VCO/DCO, Out’(t)** is a frequency locked signal which is provided to **Phase Control**. The output of **Phase Detect** is provided to **Logic2**. **Logic2** generates a phase control signal which decides whether to increase or decrease phase delay and is provided to **Phase Control**. **Phase Control** will add or subtract delay to the **VCO/DCO** output signal $Out'(t)$ accordingly and output a frequency and phase locked signal $Out(t)$.

**Figure 2 embodiment of block diagram for the frequency locked loop according to the present invention.**

In FIG 2, **TDC1** and **TDC2** comprise two identical counters which will be reset at $Ref(t)$ and $Div(t)$ rising edges respectively, then start to count **CLK** and stop at $Ref(t)$ and $Div(t)$ falling edges respectively. Referring to FIG 4, at the end, **TDC1**’s output is the **CLK** pulse numbers counted during **D1**, **TDC2**’s output is the **CLK** pulse numbers counted during **D2**. In this way, high resolution time to digital conversions are achieved ( **D1** and **D2** can have phase difference ).
FIG 2 provides an embodiment of block diagram for the frequency locked loop according to the present invention.

Digitised $D_1$ and $D_2$ are provided to SUB1. SUB1 subtracts $D_1$ with $D_2$ and output an absolute value of the difference, $Er_1$ as a frequency error and generates an $EN_2$ high when $Er_1$ first time becomes zero. $Er_1$ is provided to Digital Add and Logic. In Logic, $Er_1$'s first rising edge will generate a start signal to initiate coarse tune / proportional frequency control and to start Counter. Meanwhile, $D/A_2$'s initial output value is set to half of its maxim value. The Counter is a pre-set, up/down counter, if the current counter value is greater than the pre-set value, the counter will count down and if the current counter value is smaller than the pre-set value, the counter will count up, otherwise, the counter will stop.

The pre-set counter value is based on target frequency and its corresponding control voltage of VCO/DCO and is set each time before coarse tune start. When counter value is equal to its pre-set value, Logic will generate a stop signal to end coarse tune and to stop counter, meanwhile generate an $EN_1$ high to COMP1 to initiate fine tune / integral frequency control. The Counter will hold its output value for $D/A_1$ to generate an output voltage $V_1$ as the result of coarse tune. $V_1$ is provided to Analog Add. After $EN_1$ becomes high, COMP1 compares $D_1$ with $D_2$, if $D_1$ is greater than $D_2$, COMP1 will generate an up signal, if $D_1$ is smaller than $D_2$, COMP1 will generate a down signal, if $D_1$ is equal to $D_2$, COMP1 will let both up and down signal be low.

The up and down signals are provided to Digital Add. In Digital Add, the previous output value $D$ is read back from $D/A_2$ and then is added / subtracted by current value $Er_1$ value according to the up / down signal respectively. The result will be used to update $D$ and to generate the next $V_2(t)$. This process will continue until $Er_1$ becomes zero or within an allowable range. The output of $D/A_2$, $V_2(t)$ is provided to Analog Add. Analog Add adds $V_2(t)$ with $V_1$ to generate a proportional and integral frequency control voltage $V_1(t)$ for VCO/DCO. VCO generates a frequency locked signal $Out'(t)$ when $Er_1$ becomes zero.

Because TDC1 and TDC2 are identical and have the same CLK, time to digital conversion error caused by CLK can be mostly cancelled by SUB1 (even with phase difference), $D_1$ becomes equal to $D_2$ will generate highly reliable frequency error $Er_1$, no additional ring oscillator is needed to generate the CLK. This will significantly simplify design while providing high resolution, small error time to digital conversion even during loop transient period.

Figure 3 is an embodiment of block diagram for the phase locked loop according to the present invention.
In FIG 3, referring to FIG 4, when EN2 becomes high, AND2 is first selected as initial delay selection. SUB2 will convert time difference between Reset1 / t1 and Reset2 / t2 into a digital static phase error Er2. The first static phase error / first Er2 value will be kept in SUB2’s register as Er0, a reference value for future comparison. Er2 is provided to COMP2. The next Er2 value will be compared with Er0, if Er2 is less than Er0, COMP2 will generate an up signal high, if Er2 is greater than Er0, COMP2 will generate a down signal high and if Er2 is equal to Er0, both up and down signals will be low.

FIG 3 provides an embodiment of block diagram for the phase locked loop according to the present invention.

FIG 4 shows signal waveform relation according to the present invention.

FIG 5 is a block diagram of the prior art Analog / Digital PLL.

FIG 6 is a graph of VCO gain.

FIG 7 is a graph of output Jitter of prior art Analog / Digital PLL.

Up and Down signals are provided to SHIFT Reg. If up event and up is high, AND3 will be selected to add delay to Out'(t), If down event and down is high, AND1 will be selected to reduce delay to Out'(t), if both up and down are low, no change will happen. Only one of the three AND gates will be selected at a time. In this way, relative phase difference between Ref(t) and Div(t) is kept close to Er0 or locked. Therefor, Out(t) is frequency and phase locked. Increasing the number of the delay stages can increase the accuracy of the phase locked loop. For PLL used as a frequency synthesiser, there is no need to reduce the static phase error Er0 to zero. But if it is necessary, the static phase error Er0 can become zero after both frequency and phase are locked by forcing VCO output being synchronised to D1’s rising or falling edge once, meanwhile, Er0 has to be set to zero too.
After frequency is locked, each time when phase is out of control range, frequency fine tune will be initiated. If there is a frequency band change, coarse tune will be initiated and a new pre-set value will be assigned to the Counter.

The diagrams depicted herein are just examples. There may be many variations to these diagrams or the steps (or operations) described herein without departing from the spirit of the invention. All of these variations are considered a part of the claimed invention.

While the preferred embodiment to the invention has been described, it will be understood that those skilled in the art, both now and in the future, may take various improvements and enhancements which fall within the scope of the claims which follow.

These claims should be construed to maintain the proper protection for the invention first described.

Claims
6. Claims

I claim:

1. Frequency and Phase locked Loops for controlling the frequency and phase of an output signal Out(t) in response to an input signal Ref(t), comprising:

   (a) A frequency feedback control loop for controlling the frequency of an output signal Out(t) in response to an input Ref(t) signal frequency according to a frequency error Er1 between its divided output signal Div(t) and input signal Ref(t) and for generating an EN2 high signal to initiate phase feedback control when frequency error Er1 becomes zero or frequency is locked.

   (b) A phase feedback control loop for controlling the phase of an divided output signal Div(t) in alliance to / to match with an input signal Ref(t) phase according to the first static phase error Er0 between its divided output signal Div(t) and input signal Ref(t) and to the phase error between the first static phase error Er0 and the subsequent static phase error Er2 and for initiating frequency integral control when phase control is out of range.
2. The apparatus of claim 1, where in said frequency feedback control loop comprises:

An open proportional control loop and a close integral control loop.

3. The apparatus of claim 2, where in said open proportional control loop comprises:

Means for changing the slop and controlling the time length of proportional control and for initiating frequency integral control when Counter’s output value is equal to its pre-set value.

4. The apparatus of claim 3, where in said means for changing the slope comprises:

To change slope by changing Divider B’s constant dividing value.

5. The apparatus of claim 3, where in said means for controlling the time length of open loop proportional control comprises:

Logic generates an EN1 high to hold proportional control and to enable frequency integral control when up/down counter’s output value becomes equal to its pre-set value.

6. The apparatus of claim 2, where in said close loop frequency integral control comprises:

Means for frequency error Er1 generation and integral control.
7. The apparatus of claim 6, where in said frequency error generation comprises:

Using a high frequency CLK from the feedback Divider A to drive two identical counters combining with logic control within TDC1 and TDC2 to achieve time to digital conversion, to generate a frequency error Er1 and to generate an EN2 high signal to initiate phase feedback control after Er1 becomes zero.

8. The apparatus of claim 6, where in said close loop frequency integral control comprises:

Means for adding or subtracting the next frequency error Er1 with previous result D and updating D.

9. The apparatus of claim 1, where in said phase feedback control loop comprises:

Means for using first static phase error of Er2 value as a reference phase error Er0 to compare with subsequent Er2 to add or subtract phase delay to frequency feedback loop’s input signal Out'(t) and output a frequency and phase locked signal Out(t).

References

* Practical Phase Locked Loop Design, 2004  ISSCC Tutorial,

Dennis Fischette, http://www.delroy.com/

* Tutorial on Digital Phase Locked Loops, CICC 2009,

Michael H. Perrott, September 2009
* First time, Every Time Practical Tips for Phase Locked Loop Design,

Dennis Fischette, 2009