Xilinx Announces SDAccel Development Environment for OpenCL, C, and C++, Delivering Up to 25X Better Performance/Watt to the Data Center

Xilinx, Inc. - November 17, 2014

Combines the first architecturally optimizing compiler, libraries, development boards, and the first complete CPU/GPU-like development and run-time experience for FPGAs

PR Newswire

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NEW ORLEANS, Nov. 17, 2014 /PRNewswire/ -- At Super Computing 2014, Xilinx, Inc. (NASDAQ: XLNX) today announced the SDAccel™ development environment for OpenCL™, C, and C++, enabling up to 25X better performance/watt for data center application acceleration leveraging FPGAs. SDAccel, the newest member of the SDx™ family, combines the industry's first architecturally optimizing compiler supporting any combination of OpenCL, C, and C++ kernels, along with libraries, development boards, and the first complete CPU/GPU-like development and run-time experience for FPGAs.
"FPGA-based technology is breaking new grounds to enable optimized compute applications," said Robert Hormuth, executive director, Platform Architecture & Technology, Office of the CTO at Dell. "Ease of programming is required to lower the barrier for adopting FPGA-based accelerators in deployment of Dell servers. Xilinx is clearly on the right path to enable developers with a software environment that will accelerate productivity for FPGA platform users."

"IBM likes the Xilinx direction for enabling software programmability for Xilinx FPGAs. The flexibility and QoR of creating optimized FPGA accelerators from C, C++ and OpenCL can accelerate IBM’s ability to bring greater value to our customers," said Brad McCredie, IBM vice president of Power Development and OpenPOWER president. "IBM believes OpenCL would benefit productivity and is working with Xilinx to adopt this technology into OpenPOWER product designs."

First Architecturally Optimizing Compiler for OpenCL, C, and C++
SDAccel's architecturally optimizing compiler delivers up to 25X better performance/watt compared to CPUs or GPUs and 3X the performance and resource efficiency of other FPGA solutions. SDAccel leverages foundational compiler technology that is utilized by more than 1,000 programmers. SDAccel harnesses the power of this compiler and enables software developers to leverage new or existing OpenCL, C, and C++ code for creating high performance accelerators, optimized for memory, dataflow, and loop pipelining in a wide range of data center applications such as compute search, image recognition, machine learning, transcoding, storage compression and encryption.

First Complete CPU/GPU Like Development Experience on FPGAs
With SDAccel, developers can use a familiar workflow to optimize their applications and take advantage of FPGA platforms with no prior FPGA experience. The integrated design environment (IDE) provides coding templates and software libraries, and enables compiling, debugging, and profiling against the full range of development targets including emulation on x86, performance validation using fast simulation, and native execution on FPGA processors. The IDE executes the application on data center-ready FPGA platforms complete with automatic instrumentation insertion for all supported development targets. SDAccel has also been architected to enable CPU/GPU developers to easily migrate their applications to FPGAs while maintaining and reusing their OpenCL, C, and C++ code in a familiar workflow.

The comprehensive SDAccel environment includes the programmer-ready IDE, C-based FPGA optimized libraries, as well as commercial off-the-shelf (COTS) platforms ready for data center use.

SDAccel libraries include OpenCL built-ins, DSP, Video, and linear algebra libraries for high performance, low power implementations. For domain specific acceleration, optimized OpenCV and
BLAS OpenCL compatible libraries are available from Xilinx Alliance member Auviz Systems, Initial COTS members include Alpha Data, Convey, Pico Computing with more being added in early 2015.

**First Complete CPU/GPU Like Run-time Experience on FPGAs**

Only SDAccel supports large applications with multiple programs and CPU/GPU like on-demand loadable compute units. Unique to FPGA solutions, and like CPU/GPUs, SDAccel keeps the system functional during program transitions. SDAccel is the only environment that creates FPGA-based compute units that can load new accelerator kernels while an application is running. Throughout application execution, critical system interfaces and functions such as memory, Ethernet, PCIe® and performance monitors are kept live. On-the-fly reconfigurable compute units allow FPGA accelerators to be shared across multiple applications. For example, operational systems can be programmed to switch between image search, video transcoding and image processing.

**Availability**

Live SDAccel product demonstrations are available at this week’s Super Computing 2014 conference, booth #3903 in New Orleans. To access the capabilities of SDAccel Early Access release, please contact your local sales representative. To learn more visit [www.xilinx.com/sdaccel](http://www.xilinx.com/sdaccel).

The product is based on a published Khronos Specification, and is expected to pass the Khronos Conformance Testing Process. Current conformance status can be found at [www.khronos.org/conformance](http://www.khronos.org/conformance).

**About SDx**

SDx is a family of development environments for systems and software engineers. SDx enables developers with little or no FPGA expertise to use high level programming languages to leverage the power of programmable hardware with industry standard processors on or off chip. To learn more visit [www.xilinx.com/sdx](http://www.xilinx.com/sdx).

**About Xilinx**

Xilinx is the world's leading provider of All Programmable FPGAs, SoCs and 3D ICs. These industry-leading devices are coupled with a next-generation design environment and IP to serve a broad range of customer needs, from programmable logic to programmable systems integration. For more information, visit [www.xilinx.com](http://www.xilinx.com).

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**November 17, 2014 - Quote Sheet**

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"As a long time Xilinx customer, we are excited about the breakthrough technology Xilinx is delivering with SDAccel," said Steve Newton, vice president & director of Keysight Laboratories, at Keysight Technologies. "We are looking forward to leveraging the product and benefit from OpenCL heterogeneous computing in our next generation products."

"Alpha Data supports the Xilinx SDAccel Development Environment for OpenCL, C and C++ with the high performance half length, low profile ADM-PCIE-7V3 Virtex-7 FPGA board," said Adam Smith, CEO of Alpha Data. "The combination of SDAccel and our board enables OpenCL application developers to obtain the best performance per watt for Data Center data processing, system modeling and market analysis applications."

"Auviz Systems provides C-based FPGA optimized libraries for developers to use with the Xilinx SDAccel Development Environment for Acceleration. Auviz used the SDAccel architecturally optimizing compiler to successfully create OpenCV libraries to increase developer productivity and get higher performance from FPGAs than CPUs and GPUs," said Nagesh Gupta, founder and CEO of Auviz Systems.

"Convey Wolverine coprocessors together with high level programming tools, like Xilinx’s SDAccel Development Environment for OpenCL, C and C++ enable high performance data center application acceleration," said Bruce Toal, CEO of Convey Computer Corporation. "FPGA-based accelerators are delivering new levels of price/performance with low power consumption for fewer system platform deployments in data centers."

"Pico Computing’s modular, highly scalable FPGA-based HPC systems support the Xilinx SDAccel Development Environment for Acceleration to deliver optimal performance across all Xilinx-supported device families for OpenCL developers working in imaging, bioinformatics, networking, academic, and other high performance computing applications," said Jaime Cummins, CEO, Pico Computing.

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