When I started my career in electronics, there weren’t many signal integrity issues related to PCBs. Heck, there weren’t many PCBs! In the beginning, you could literally layout a PCB with an X-Acto knife, and do the chemistry in the kitchen sink. Some of us remember that RF (at that time) was 1.0 megahertz, right in the middle of the AM broadcast band. Since then, PCB technology has become ever more complex, and circuit speeds have become faster and faster, so that today, signal integrity issues are a routine concern for many (if not most) of us.

In my mind, the signal integrity issues as related to PCBs have progressed through four stages. Those stages are listed below. The first one is trivial, and I list it only for continuity purposes. The rest of the blog will describe the other three.

Stages in the progression:

Stage 1:

No signal integrity issues.

Stage 2:

Issues caused by, or related to inductance.

Stage 3:

Issues caused by the fact that resistance is no longer a constant with frequency, but it varies as a function of frequency.

Stage 4:

Critical lengths are now so short that it is extremely difficult to implement solutions, even if the problems are known.

Root cause of the progression: There is a single parameter that is driving the industry from one stage to the next. That is faster and faster rise times.
Stage 2: Inductance:

The inductance of traces on PCBs is pretty low. Normally we do not have to be concerned about the inductance associated with a trace until the rise time of the signal gets really short. How short? Well, the formula for the voltage caused by inductance is pretty straightforward:

\[ V = L \frac{di}{dt} \]  

(Eq. 1)

People who have taken calculus will recognize this expression. If you have not, then assume the “d” stands for “delta,” or “change.” V is the induced voltage, L is the inductance, di is the change in the current (i.e., the switched current), and dt is the rise (or fall) time of the signal. On a PCB, L is pretty small, as small as 10^{-8} or 10^{-9} Henrys. Even di is pretty small, unless we start talking about hundreds of thousands of transistors switching at the same time, as in a large microprocessor. So V would be small unless dt is also very small. If we are talking about a rise time of a nanosecond, then dt is 10^{-9}, and suddenly V begins to matter! So the answer to “How small?” generally depends primarily on the rise time of the signal and secondarily on the amount of current being switched.

The root cause of inductance is the changing magnetic field caused by a changing current flow. It is the inductance itself, or the changing magnetic field related to the inductance, that causes most of the effects in Stage 2. Effects fall into one of four categories, EMI, crosstalk, ground bounce on the power distribution system, or signal reflections.

Although there are those who would disagree with me, I argue that EMI and crosstalk are fundamentally the same thing. If the victim trace is far away we call it EMI; if it is close by we call it crosstalk. Both are caused by the electromagnetic coupling caused by the inductive current loop of the signal during very fast switching times (with really no need to talk about whether we are concerned about near field or far field effects.) And the solution to EMI and crosstalk are the same: route the traces as close as possible to a continuous, related underlying plane, and separate the aggressor and victim traces as far as possible. Since EMI can also be caused by inductive noise loops on planes, an additional solution for EMI is the use of power and ground return plane pairs for planar capacitance.

Ground bounce is caused when a fast switching current sees some inductance. For example, if a logic gate switches between logic levels, there is a sudden change in current. If thousands of gates switch simultaneously, there can be a pretty healthy change in current. And this change can happen in less than a nanosecond. If there is inductance in that path (say at the pad where the IC connects to the PCB) then a sudden noise voltage spike can exist at that point. That in turn can (and probably will) add to the signal voltage. So the next logic gate in the signal path sees not only the signal but also a noise spike superimposed on top of it. If the noise spike is great enough, logic errors can result. (You will note that I am describing the phenomena known as “ground bounce” here.)

The solution to this problem is the design of an adequate Power Distribution System (PDS). Fundamentally, it involves the judicious use of bypass capacitors, low inductance vias and pads, and power and ground plane pairs for planar capacitance.

Reflections are indirectly related to inductance. When any signal propagates down a trace, it reflects back (except in one very special case.) The fundamental question is whether or not we care about the reflection. If the reflection interferes with the signal (as in interfering with the subsequent bits being sent down the trace) then we care. But if the reflection is not going to interfere, then we don’t care. Whether or not we care generally depends on the relationship between the rise time of the signal and the propagation time of the signal down the trace (and back.) If the signal comes back really quickly (before subsequent bits are transmitted) then we probably don’t care. But if it takes a
relatively long time for the reflection to get back, then we might care.

We often talk about the “critical length” of a trace. The critical length is usually (it is not a precise concept) considered to be the length where the “round trip” propagation time (down and back) is equal to the rise time of the signal. For traces shorter the critical length, we usually don’t need to worry about the reflections. For traces longer than the critical length, we might want to take the possibility of damaging reflections into consideration.

The solution to the reflection problem is to use controlled impedance traces, and then terminate them in their characteristic impedance. Controlling the impedance of a trace means controlling the inductive path of the current loop. That is done with the geometry of the trace. Fundamentally, it involves controlling the width of the trace and its separation from its continuous, relevant underlying plane (and also controlling the dielectric properties of the material between the trace and the plane.)

We'll cover Stages 3 & 4 in Part 2 of this blog.