FPGA-based FSK/PSK modulation

Ahmed Asim Ghouri - December 11, 2014

Binary FSK (Frequency Shift Keying) and PSK (Phase Shift keying) are extensively used in telecommunication for digital data transmission. FSK/PSK modulator circuits usually employ analogue components such as VCO (voltage control oscillator), RF Mixer, and Level-shifter, with limited frequency range and whose performance drifts with variation in environmental temperature and duty cycle. An FPGA-based all-digital implementation ensures constant optimum performance and reconfigurability.

This article discusses practical application of a combined Binary FSK and PSK modulator. It highlights how embedded resources can be used to implement an all-digital FSK / PSK modulator, which modulates serial data transmission of a UART (Universal Asynchronous Receiver and Transmitter). In this application the modulation scheme targets Altera’s Cyclone-IV FPGA populated on a DE2-115 development board from Terasic and an HSMC (High Speed Mezzanine Card). A system block diagram shows how a LUT based NCO is used to generate the sine wave with varying frequency and then with varying phase. Extensive testing and its results are discussed to verify the modulation.

Frequency Shift Keying Modulation

Frequency-shift keying (FSK) is a frequency modulation scheme in which digital information is transmitted through discrete frequency changes of a carrier wave. The simplest FSK is binary FSK (BFSK). BFSK literally implies using a pair of discrete frequencies to transmit binary (0s and 1s) information. With this scheme, the "1" is called the mark frequency and the "0" is called the space frequency. The time domain of an FSK modulated carrier is illustrated in the figure 1 below.

![Figure 1](image1.png)
The figure 2 below is the system for switching the transmitter according to the modulating signal level. If the switching timing in the synchronization and modulating signal of the two oscillators is not good, the continuity of the phase between bits cannot be maintained as shown in the figure, resulting in an unnecessary spectrum that is not in fact used. The out-of-band unnecessary spectrum interferes with adjacent channels, and this spectrum is called a spurious emission.

Figure 2

Phase Shift Keying Modulation

Phase-shift keying (PSK) is a method of digital communication in which the phase of a transmitted signal is varied to convey information. There are several methods that can be used to accomplish PSK. The simplest PSK technique is called binary phase-shift keying (BPSK). It uses two opposite signal phases (0 and 180 degrees). The digital signal is broken up time wise into individual bits (binary digits). The state of each bit is determined according to the state of the preceding bit. If the phase of the wave does not change, then the signal state stays the same (0 or 1). If the phase of the wave changes by 180 degrees -- that is, if the phase reverses -- then the signal state changes (from 0 to 1, or from 1 to 0). Because there are two possible wave phases, BPSK is sometimes called biphase modulation. The time domain trace of an PSK modulated carrier is illustrated in the figure 1.1 below.
DE2-115 Board

The Cyclone EP4CE115 device equipped on the DE2-115 features 114,480 logic elements (LEs), the largest offered in the Cyclone IV E series, up to 3.9-Mbits of RAM, and 266 multipliers. In addition, it delivers an unprecedented combination of low cost and functionality, and lower power compared to previous generation Cyclone devices. The DE2-115 adopts similar features from the earlier DE2 series primarily the DE2-70, as well as additional interfaces to support mainstream protocols including Gigabit Ethernet (GbE). A High-Speed Mezzanine Card (HSMC) connector is provided to support additional functionality and connectivity via HSMC daughter cards and cables. For large-scale ASIC prototype development, a connection can be made with two or more FPGA-based boards by means of a HSMC cable through the HSMC connector. Figure 4 shows block diagram of DE2-115 board.

High Speed Mezzanine Card (HSMC)

The Data Conversion HSMC was created to provide a set of Analog to Digital and Digital to Analog interfaces including an Audio Codec interface.

The Data Conversion HSMC contains the following components.

Interfaces

1. HSMC Interface
2. Audio CODEC Interface
3. External Clock In Interface
4. External Clock Out Interface
5. ADC Channel A and B Input Interface
6. DAC Channel A and B Output Interface

Power supply

I2C Serial EEPROM

Block diagram shown in figure 5 shows the components on HSMC card and their interfaces.

![Block diagram](image)

**Figure 5**

**FPGA Implementation of FSK Modulator**

Here we will be targeting a Cyclone-IV FPGA on development board DE2-115 for the implementation of FSK Modulator. The basic modules required for this implementation are:

1. UART (Universal Asynchronous Receiver and Transmitter)
2. Numerically Controlled Oscillator (NCO)
3. Phase Locked Loop (PLL)
4. UP-Counter
5. High Speed Mezzanine Card (HSMC)
The figure 3 below shows how these modules are connected.

![Figure 3](image)

**Figure 3**

**Binary FSK Modulation VHDL Description**

As shown in figure 3 within this FPGA implementation PLL is being used to supply clean synchronized clock to UART, NCO and UP-Counter, whereas MUX_1 selects which frequency is set for the LUT-based NCO, the select signal is toggled by a MUX_4 output. User SW[17:0] selects whether to enable FSK Modulation by setting select lines to logic “0” of MUX_4 or enable Binary PSK Modulation by setting select lines to logic “1”. Binary Data is transmitted by a UART which is transmitting a pre-defined binary value in continuous loop at the rate of 9600 baud rate. When TX output drops to “0” NCO is set to generate 6Mhz sinewave and when it pulls up to logic “1” NCO is generating 12Mhz sinewave. The output of the NCO and the UP-Counter are selected by user via switches SW[17:0] using MUX_2, here UP-Counter is being used for testing purpose only. When a UP-Counter is selected the output of DAC will be a saw-tooth wave, whereas NCO’s output will result in a sine wave. The output of MUX_2 is fed to a high-speed DAC populated on a HSMC card. There are two 14-bit DAC’s available on HSMC card one on channel A and the other on channel B, each has the conversion rate of 250Ms/ps. The analogue output of both DAC’s terminates on a surface mount SMA connector.

**Binary PSK Modulation VHDL Description**

Refer to figure 3 When user sets SW[17:0] to enable PSK Modulation MUX_4 output is logic “0” which sets NCO to generate 6Mhz of Sine and Cosine wave. UART serial output TX is routed via
MUX_3 to MUX_2. The DAC "A" analogue output shifts its frequency synchronously with the bit toggling from the output of MUX_3, which in turn change the channel selection of MUX_2.

**VHDL Description**

The implementation of blocks shown in figure 3 are described in VHDL in the following list of files:

1. Hsmc_card_interface_Top.vhd
2. UART_TX_CTRL.vhd
3. GPIO_demo.vhd
4. gh_nsinicos_rom_14_4.vhd
5. gh_nco_lut_14p.vhd

**Top VHDL File**

The top vhdl file combines all components and contains interface description and signals for the DE2-115 board to HSMC card.

Download [Hsmc_card_interface_Top.vhd](#) file. Download complete [Quartus project](#).

**Main Processing**

The process labeled "Interfacing_ADC_DAC" in the top entity as shown above has been divided into 6 conditional functions. It starts with resetting output ports DA and DB that are connected to DAC_A and DAC_B, similarly ADC registers ADC_data_A and ADC_data_B.

**1st Condition**

First condition detects user input from switches SW[17:15] and connects ADC ‘A’ and ‘B’ 14-bit inputs to internal 14-bit registers ADC_data_A and ADC_data_B and DAC ‘A’ 14-bit output to UP-Counter whereas DAC ‘B’ output to inverted bits of UP-Counter if SW[17:15] = “000”.

**2nd Condition**

Second condition detects user input from switches SW[17:15] and connects ADC ‘A’ 14-bit input port to DAC ‘A’ output port and whereas DAC ‘B’ output port to ADC ‘B’ input port if SW[17:15] position is set to “001”.

**3rd Condition**

Third condition detects user input from switches SW[17:15] if these are set to "010" it connects 14-bit NCO’s sine wave output added with a offset value to out port of DAC ‘A’ and DAC ‘B’. NCO is generating sine wave set by default value i.e 12Mhz initially set during reset when detecting reset_n = '0'.
4th Condition

Fourth condition detects user input from switches SW[17:15] if these are set to "100" it connects 14-bit NCO’s sine wave output added with a offset value to out port of DAC ‘A’. Externally DAC ‘A’ analogue output from SMA connector is connected by a RF cable to analogue input of ADC ‘A’, the converted 14-bit output of ADC ‘A’ is fed to DAC ‘B’. This condition can be used to evaluate the performance of DAC and ADC.

5th Condition

Fifth condition detects user input from switches SW[17:15] if these are set to "101", it assigns internal Freq_set register to 12Mhz when UART TX output is at logic “1” and 6Mhz when TX output is at “0”. Simultaneously it connects NCO output to DAC ‘A’, the analogue output of DAC ‘A’ which terminates at SMA connector can be observed on the scope to monitor FSK modulation.

6th Condition

If switches SW[17:15] are set to "110", DAC ‘A’ output port is connected to Sine wave NCO output when UART_Txout is at logic “1” on UART_Txout toggling to logic “0” DAC ‘A’ output port is connected to Cosine wave output of NCO, thus generating Phase Shift Keying modulated wave. UART TX output is also routed to UART_TXD pin of UART on DE2-115 for testing purposes.

Test Set-up

Pictures below show DE2-115 based test setup for testing Binary FSK and PSK modulation testing described in the top entity “Hsmc_card_interface_Top”. Hsmc Card is connected to DE2-115 board via Hsmc port with 160 pins, refer to DE2-115 Schematic from Terasic for more details. Picture shows a RF cable connected to surface mount SMA connector of DAC “A” analogue output.
**Testing 1st condition:** The picture below shows oscilloscope screen capture of 1st condition, its shows output of DAC “A”. It shows analogue output of the DAC translating 14-bit Up-Counter values.

**Testing 3rd condition:** The picture below shows oscilloscope screen capture of 3rd condition, its shows output of DAC “A” which is a pure sine wave of 12Mhz.
Testing 5th condition: The pictures below shows oscilloscope screen captures of 5th condition, its shows Binary FSK modulated output of DAC “A”. Channel 2 trace shows the rising edge of the UART TX output whereas Channel 1 trace shows change in frequency from 6Mhz to 12Mhz. Second picture shows shift in frequency from 12Mhz to 6Mhz in reference to the falling edge of the TX output. Third screen shot shows FFT trace of the oscilloscope, clearly shows peaks at 6Mhz and 12Mhz.

Binary FSK Modulation on rising edge of UART TX
Binary FSK Modulation on falling edge of UART TX

Testing 6\textsuperscript{th} condition: The pictures below shows oscilloscope screen captures of 6th condition, its shows Binary PSK modulated output of DAC “A”. Channel 2 trace shows the rising edge of the UART TX output whereas Channel 1 trace shows change in Phase of 6Mhz sine wave. Second picture shows Phase reversal in reference to the falling edge of the TX output. Third screen shot shows FFT trace of the oscilloscope, clearly shows peak at 6Mhz only.
Binary PSK Modulation at Rising Edge of TX output

Binary PSK Modulation at Falling Edge of TX output
FFT trace of Binary PSK Modulation at 6Mhz

FFT Trace of FSK Modulation on 7th condition, modulating Countreg(18) i.e 6.1Khz Square Wave

The author is with Embedded Strings Inc., which specializes in the design, development, testing, and manufacturing of complex embedded systems/hardware.