Stage 3: Resistance as a function of Frequency:

Most of us have understood that resistance is constant with frequency. It is only inductive or capacitive reactance that varies with frequency. That is true, up to a point. But there comes a time when the resistance of traces on PCBs does start to change as a function of frequency.

The reason this happens is twofold. First, the skin effect begins to come into play. Skin effect reduces the apparent cross sectional area of the trace at higher frequencies. Since the resistance of a conductor is inversely proportional to its cross-sectional area, the resistance of the trace increases for higher frequencies. Clock and data signals are not single-frequency sine waves. Instead they more closely resemble square waves and carry many harmonics besides the fundamental frequency. The higher harmonics face higher resistance than do the lower frequency harmonics, so the waveform is distorted as it travels along the trace. For those of you familiar with eye diagrams, the manifestation of this problem is a closing of the eye.

The second problem is dielectric loss. Think of the dielectric as consisting of a gazillion atoms grouped together in molecules. Inherent in this structure are electrons surrounding the atoms. The electrons are attracted to positive charges and repelled by negative charges. Alternating current acts like alternating charges (caused by the changing electric field around the trace). The electrons are in constant motion, alternatively being attracted to and repelled by the signal as it propagates down the trace. The actual movement is miniscule. But there is a force exerted on the electrons that tries to move them. A sort of friction holds them in place, and the combination of the forces and the friction results in heat. It is a form of power loss.

Now, where does the power come from? The signal. A little bit of power is absorbed from the signal because it is lost to the internal friction in the dielectric. Because this effect is stronger at higher frequencies, the higher frequency signal harmonics lose more power than do the lower frequency signal harmonics. The net effect is the same as with the skin effect: the higher frequency harmonics of the signal are attenuated with respect to the lower frequency harmonics. In fact, from a signal measurement standpoint, it is almost impossible to separate these two effects (although we can do so theoretically quite well).

The solution to this signal integrity problem is to restore the balance between the lower frequency harmonics and the higher frequency harmonics. We can do that by amplifying the higher frequency harmonics (with an amplifier), or attenuating the lower frequency harmonics (with a passive filter). And we can do either at the beginning of the trace (pre) or at the end of the trace (post). This results in four possibilities, pre- or post-, active or passive equalization.
The board designer plays only a minor role here. The real responsibility lies with the circuit design engineer who must select the type of equalization scheme to use (active or passive) and where to place it (pre or post). The board designer then implements that decision.

**Stage 4: Very Short Critical Length:**

Perhaps you are already aware that the generally accepted critical length for a 1.0 nanosecond rise time (approximately 300 MHz signal) is 3 inches. It works out that the critical length for a 5 GHz signal (75 picosecond rise time or so) is on the order of a quarter of an inch. There is simply not enough room to place effective trace terminations, pads, and vias in such a short region. So the question becomes, what can we do when we get to these very short critical lengths?

While the industry has rules of thumb that are generally accepted for solutions to Stage 2 and Stage 3 issues, we are not all totally agreed as to what to do with stage 4 issues. One way to see that is to look at the conflicting design rules that are issued by different component suppliers as written in their application notes and as written by different authors in different articles. A great deal of attention is being paid to standardizing well behaved low-inductance controlled-impedance pads and vias, and to component and even package design. In any event, stage 4 is where today’s action is. If your designs have not reached this stage yet, perhaps you are lucky. But someday they will.

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