Series-connected MOSFETs increase voltage & power handling

Ilija UzelacRon Reiserer, - January 05, 2015

This Design Idea presents a simple, proven, reliable, and robust method for charging large capacitor banks, using a series connection of power MOSFETs to raise the breakdown voltage over that of an individual MOSFET.

When a power supply drives a large capacitive load, inrush current, if not limited, can reach tens or hundreds of amps for a high voltage power supply. In general, maximal ratings of a power supply could be transiently exceeded by many times, but this is generally acceptable when the transient lasts a few AC-line cycles. This is typical for load capacitances up to a couple of hundred microfarads, but for load capacitances in thousands of microfarads, an inrush current limiter is a must.

Using MOSFETs as voltage controlled current elements is very suitable to capacitor-charging circuit design. Consider though: If a task specifies charging a capacitor bank with 1A from rectified AC mains of 240V, a design with a single P-MOSFET would require that at power-on, the MOSFET pass 1A when its drain-to-source voltage |V_{DS}| is about 330V, which exceeds the safe operating area of most parts. For example, the IXTQ10P50P, at the maximum junction temperature of 150°C, can handle 200 mA when |V_{DS}| = 250V, but over 2A when |V_{DS}| < 100V. This limitation can be overcome by connecting multiple P-MOSFETs in series.

Figure 1 shows a design with three P-MOSFETs connected in series. Neglecting the voltage drop...
across R1, the input voltage is approximately the same as the potential at Q2’s source. Then, the gate potential of Q2 equals the input voltage minus 6.2V across Zener D1, and plus any voltage drop across resistor R3. Resistors R5, R6, and R7 as voltage dividers ensure that the $|V_{DS}|$ of each P-MOSFET is approximately equal – about 1/3 of the voltage difference between the input and output. R5 is purposely chosen to have a slightly higher resistance than R6 and R7 as the gate potential of Q2 is about 5V less than the input voltage. This correction equalizes $|V_{DS}|$ voltages even more than if resistors R5, R6, and R7 were equal. R4 ensures that at power-on/off, Q2 is turned off.

At power-on, D1 provides 6.2V between the source and gate of Q2, $|V_{GS2}|$; therefore Q2 is conductive. Q3 and Q4 are conductive as well, as the current through R5-R7 charges their gate-to-source capacitances. The capacitor bank charging current is sensed with R1 and regulated with the negative feedback control consisting of R1, Q1, R3, and Q2. When the voltage between the emitter and base of Q1 reaches $V_{BE(on)}$ – that is, when the charging current is about 1A – Q1 starts to conduct. As $|V_{GS2}| = 6.2 - R3 \times I_{C(Q1)}$, any increase in $I_{C(Q1)}$ decreases $|V_{GS2}|$. This decreases the output current, which in turn decreases the voltage across R1, completing the negative feedback loop.

**Figure 2**

Figure 2 shows voltage across the 40,000µF capacitor bank as a function of time as the capacitor bank is charged from 0V to 300V – for two different cases – with and without C1. Without C1, the capacitor bank is only partially charged during each rectified half-cycle – that is, when the input voltage is higher than the output voltage plus the voltage drop across all three MOSFETs of about 15V. Hence, the slope of the curve is not constant.

Adding C1 lets the charging circuit work with a more constant input voltage.

**Calculations for C1**
C1 discharges at the rate of $\frac{dV}{dt} = \frac{I}{C} = 10\text{V/ms}$. This is almost order of magnitude slower than the sinusoidal change of the input voltage from 330V to 0V that lasts 4.17ms for 120Hz half-cycles. Therefore, from the moment the input voltage reaches its maximum, the capacitor bank is charged only from the C1 capacitor until the input voltage exceeds the C1 voltage on the next rising slope of the 120Hz period. As C1 is discharged with the constant current of 1A, the discharge time interval $t_d$ is expressed as:

$$t_d = \frac{C}{I} (V_{\text{max}} - V_{C1}) \quad (1)$$

For this time interval, the input voltage changes from 330V to 0V and up to $V_{C1}$:

$$t_d = 4.17\text{ms} + \frac{1}{2\pi 60\text{Hz}} \arcsin \left( \frac{V_{C1}}{V_{\text{max}}} \right) \quad (2)$$

Solving these two equations for $V_{C1}$ shows that C1 discharges down to about 265V. As the voltage drop across three MOSFETs is about 15 V, it follows that above 250V, the voltage across the capacitor bank doesn’t increase linearly. This explains the variation from the linear dashed line in Figure 2.

This circuit is part of a complex device: our custom-built defibrillator for research studies [1]. It has proven to work reliably for hundreds of cycles and hundreds of hours with numerous rapid discharges of the capacitor bank over the last two years. The circuit is tested up to an input voltage of 280 $V_{\text{rms}}$ and works reliably with a heatsink temperature of up to 70°C. This Design Idea is not limited to the input voltage and current specified herein. The maximum input voltage and charging current can be raised with the addition of more P-MOSFETs in series. The downside is the voltage drop across each P-MOSFET of about 5V. Larger C1 capacitances than 100µF would linearize the charging curve at even higher voltages, or, of course, a DC input could be used.

References: