I'm frequently asked why I refer to the effective inductance of a voltage reference, voltage regulator, or op-amp in my articles. Others question "Is there really an inductor in there?", "Where does this inductance come from?", and "Why is the inductance so load current dependent?" I'll answer all of these questions.

There are several different common circuit structures that employ voltage-feedback loops within voltage references, voltage regulators, and op-amps. A simplified schematic of one such topology, shown in Figure 1, serves to illustrate the general relationships presented in this article. Other topologies such as the PNP low dropout regulator or shunt regulator have similar results and can be derived in a similar fashion. Figure 1 can represent an IC or a discrete voltage regulator.

![Figure 1. Functional structure of a common series type linear regulator or voltage reference.](image)

The typical "pass" element represented as BJT1 can be a silicon BJT transistor or MOSFET-based output stage and is used to provide the current gain of the device. These output stages can include a bulk series resistor, shown here as Ro, which is used for current-limit protection internal to the regulator or as the resistance of the pass element junction. Because the BJT is simpler to evaluate, I'll base the math on it.

During typical operation of the regulator, transistor BJT1 presents a small signal emitter resistance, Rj, that is dependent on the junction current, Ij, in accordance with Shockley's diode equation.
Where $N$ is the emission coefficient, typically 1 for a bipolar transistor (though significantly different for a MOSFET or diode), $T_k$ is the temperature in Kelvin, $I$ is the junction current, $k$ is Boltzmann's constant, and $q$ is the elementary electron charge. The resulting small-signal junction impedance, $R_j$, is the familiar small-signal relationship, $26 \text{ mV}/I_j$, and this dynamic resistance appears in series with the fixed bulk resistor, $R_o$, which includes the series resistance of the transistor emitter junction.

Referring to Figure 1, an op-amp amplifies the error voltage between a precision voltage reference, $V_{\text{ref}}$, and the output voltage, which is connected to the op-amp through a resistor, $R_1$. The amplifier output then drives the output stage, creating a closed loop circuit. The amplifier circuit generally includes frequency compensation to assure the stability of the loop, often referred to as $C_c$. This on-chip capacitor also provides dominant-pole compensation consistent with most voltage regulators and voltage output devices as stated earlier. In most cases, the frequency compensation capacitor is internal to the device. Some devices may also include a compensating zero that allows very low ESR (equivalent-series resistance) capacitors to be used, but the simplest case to evaluate is the single pole compensator. VCVS represents the op-amp. The voltage reference is SRC4.

The transfer function of the open-loop gain vector, $T$, of the amplifier using a single dominant pole control loop is defined by:

$$T = \frac{Ga}{s + a} \quad \text{(Eq. 2)}$$

Where $a$ is the corner frequency or pole location of the internal dominant pole created by $C_c$, in radians. The open-loop DC gain is represented as $G$, which is 5000. The simulated loop gain for the case of Figure 1 is shown in Figure 2.
Figure 2. Bode plot showing the phase and gain traces. This magnitude plot indicates the location of the dominant pole, "a" at 100 Hz (m2) and also the DC gain, G at 5000 (m1).

The frequency dependent closed-loop output impedance of the regulator is defined by the open loop resistance, $R_o + R_j$, and the control-loop gain vector, $T$.

$$Z_{reg} = \frac{R_o + R_j}{1 + T} \quad \text{(Eq. 3)}$$

Substituting Eq. 2 into Eq. 3 results in the closed loop impedance $Z_{reg}$.

$$Z_{reg} = \frac{(R_o + R_j) \cdot (s + a)}{a \cdot (G + 1) + s} \quad \text{(Eq. 4)}$$

The closed-loop impedance, based on the known circuit parameters, can be separated into three regions. The first region is the DC term, representing the closed-loop DC resistance. The second region is an AC-dependent impedance, and the third region reflects the amplifier's large, but finite, DC gain.

The DC closed-loop output resistance of the regulator can be evaluated using Eq. 4 by setting the frequency related parameter, s, equal to zero and simplifying. The DC output resistance is shown in
The AC output resistance can be easily obtained by differentiating Eq. 4 with respect to the frequency related parameter, \( s \), resulting in:

\[
Z_{reg\_AC} = \frac{d}{ds} \left[ \frac{(Ro + Rj) \cdot (s + a)}{a \cdot (1 + G) + s} \right] 
\]

\[\text{(Eq. 6)}\]

\[
Z_{reg\_AC} = \frac{Ro + Rj}{a(G + 1) + s} - \frac{(Ro + Rj) \cdot (s + a)}{(a(G + 1) + s)^2} 
\]

\[\text{(Eq. 7)}\]

It's interesting to note that the AC impedance in Eq. 7 has an \( s \) in the numerator, and so it can be equated with an inductor. This network can also be represented in a still simpler way using partial fractions as a series resistor and an inductor with a parallel resistance appearing due to the finite gain, \( G \).

\[
L = \frac{Ro + Rj}{a(G + 2)} \]  
\[\text{(Eq. 8)}\]

The parallel resistor can be determined by evaluating Eq. 4 with the frequency related term, \( s \), approaching infinity.

\[
R_{parallel} = Ro - \frac{(Ro + Rj)}{G + 1} \]  
\[\text{(Eq. 9)}\]

The regulator impedance can, therefore, be represented by three terms as:

\[
Z_{reg} = Z_{reg\_DC} + \frac{(L \cdot s) \cdot R_{parallel}}{(L \cdot s) + R_{parallel}} \]  
\[\text{(Eq. 10)}\]

The relationship between load current and the effective inductance can be seen by substituting for Eq. 1 for \( R_j \).

\[
L = \frac{Ro + \frac{N \cdot k \cdot T_k}{q \cdot I_j}}{a(G + 2)} \]  
\[\text{(Eq. 11)}\]
Using the example of Figure 1, with $S=628$ radians/sec (100 Hz) and $G=5000$, the simulated output impedance is shown for three different output currents in Figure 3.

**Figure 3.** Closed-loop output impedance for three different load currents, illustrating the load current dependency. As the dynamic junction resistance gets small compared with $R_o$ the current dependency is greatly reduced, as seen here. The +6dB/octave region confirms the inductive nature of the closed loop.

The impedance calculated using the exact solution of Eq. 4 and the impedance calculated using the partial fraction result of Eq. 4 are plotted together in Figure 4, which confirms that the two solutions are equivalent.
Figure 4. The result of Eq. 4 (red solid trace) and the partial fraction result of Eq. 10 (blue dotted trace) confirm the equality of the two equations.

Output impedance measurements, performed on a voltage reference at two different currents, are shown in Figure 5. These measures results clearly show the three impedance regions, as well as the sensitivity to operating current.

Figure 5. Voltage reference output impedance at two operating currents shows the sensitivity to output current and also shows the 3 distinctive impedance regions.

Also see
Match impedances when making measurements
Impedance measurements stabilize op-amp buffers
How to measure the world's fastest power switch