Wideband AFE based on a continuous-time high speed delta-sigma ADC

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Continuous time delta-sigma (CTDS) ADC is the architecture of choice for audio systems, for phone handsets and for mobile electronics. This ADC architecture allows efficient integration, signal chain reduction, low power consumption among other benefits. While CT DS ADCs outperform other classes of ADCs when high dynamic range and power efficiency are the primary requirements, other types of ADCs, such as pipelined ADCs, have been the mainstream choice for cellular communication infrastructure systems, thanks to their ability to convert very wide band analog input signals.

Recent technology breakthroughs introduced at Analog Devices are now allowing CT DS ADCs to digitize wideband signals at very high frequency. That overcomes previous limitations and enables, also in wider band systems, the significant system level benefits introduced by CT DS ADCs and that made them pervasive in lower frequency applications.

This article describes an implementation of such recent innovations. In particular an analog front end, including at its core a wideband CT DS band-pass ADC, for the digitization and down conversion of high frequency signals in communication and instrumentation systems is discussed. The embedded band pass ADC does not require an external anti-aliasing filter and driving amplifiers/buffers, substantially reducing the signal chain’s component count, power consumption and relaxing its overall specifications. Moreover on-chip programmable digital filtering and down conversion are also integrated, providing a complete and easy to use solution to the designer.

Continuous-time delta-sigma (CTDS) ADCs[1] have been the analog-to-digital architecture of choice in broad set of applications ranging from high performance audio to cellular handset RF front-ends for several years owing to a number of advantages over other types of ADCs. The benefits include greater amenability to integration and low power consumption, but also, and possibly more importantly, because using a CTDS solves a number of significant system level problems. Due to a number of technology shortcomings, the use of CT DS has been previously limited to relatively lower frequency/bandwidth, lower dynamic range. Therefore, so far, high performance Nyquist rate converters, such as pipelined and successive approximation ADCs, have been the mainstream solution for high performance/high frequency digitization applications.
However, recent technology breakthroughs introduced at Analog Devices have allowed overcoming many prior limitations. Hence making [high speed ADCs](#) based on CT DS able to achieve substantially higher performance specifications, stability in the presence of strong interferers, programmable frequency response and, in turn, enabling the solution of a number of important signal processing problems in cellular infrastructure systems and selected high performance instrumentation applications among others.

**Classic heterodyne receive signal chain**

To better understand that, let us consider, for example, a classic heterodyne receive signal chain for a communication system. A traditional scheme using a mainstream switched capacitor Nyquist-rate high speed ADC is depicted in Figure 1(a). Here, the intermediate frequency (IF) signal produced by the mixer needs to be buffered and possibly amplified using a driving amplifier. The Nyquist ADC also requires an anti-aliasing filter (AAF), sometimes implemented by a surface acoustic wave (SAW) filter or a multi-pole discrete SMD filter. Finally the desired IF radio signal reaches the ADC. Its output, clocked at a high sample rate fs (with fs/2 substantially larger than the center/IF frequency), is further processed (e.g. filtered and down-converted to base band) by a communication digital ASIC.

The same processing chain dramatically simplifies when using a CT DS as shown in Figure 1(b). Since the CT DS has a resistive input, that can be driven directly by the mixer and does not require a driving amplifier. Moreover, the CT DS’s inner core includes a CT analog filter which implicitly performs the AAF function and hence allows doing away[2] with the input SAW/SMD discrete filter. Furthermore, the CT DS can have a band-pass filter frequency characteristic (see Figure 2 for an example of actual measurements), tunable to center at the desired IF input frequency and with a significant out-of-band attenuation. Such pass band is oversampled, digitized, it is digitally decimated and down-converted to based band and provided to the digital ASIC at a much lower data rate (and with lower power consumption) than in the case of Figure 1(a).

**Figure 1: A classic heterodyne receive signal chain for a communication system implemented using (a) a traditional scheme with a Nyquist-rate switched capacitor ADC and (b) using a continuous time delta-sigma ADC.**

**Figure 2: Experimental digitized output (blue solid line) from a band-pass CT DS with an input single tone at 1GHz, bandwidth set for 75MHz and centered at 1GHz, noise bandwidth of 366.2KHz. The DS frequency-shapes the conversion quantization noise, to be low (higher dynamic range) within the pass-band of interest (while its power is higher out of band). The notch of the band-pass frequency characteristic is clearly visible in the upper plot (centered at 1GHz and 75MHz wide). The superimposed red dashed line indicates the corresponding signal transfer characteristic with visible flatness well over the desired input band. The lower plot shows a zoomed-in detail of the 75MHz wide in-band. The latter**
is subsequently digitally filtered with very high selectivity (rejecting all together the out of
band content, including the higher noise floor, any out of band distortion and out of band
blockers, on the left and right hand sides of the 75MHz wide band) and down-converted to
base band before being returned at the output of the CT DS.

The above described system level simplification is the direct result of fundamental architectural
differences between CT DS and other high speed ADC architectures.

Additional benefits of this simplification

The additional benefits of this simplification are substantial. In Figure 1(a), the driving amplifier can
consume a comparable power as the ADC itself while impacting the overall noise figure of the chain.
The AAF in Figure 1(a) cannot be easily integrated. Moreover, a new filter needs to be suitably
selected for each choice of IF (and frequency plan) and specific signal chain implementation.
Experienced system designers know well that the implementation of the filter can often be very time
consuming as different component selections, with the same filter function, can lead to dramatically
different linearity performance due to the nonlinear interaction with the front end sampling circuitry
of the Nyquist ADC.

Conversely, in Figure 1(b), where the AAF filter is removed and a front-end sampling circuitry is
replaced by the CT DS’s benign resistive input, the filtering function is performed by the CTDS and
its frequency characteristic has been made digitally programmable in Analog Devices’ technology.
Therefore, the very same CT DS can be interchangeably used in multiple signal chains and digitally
tuned to the desired frequency and bandwidth, greatly simplifying and accelerating the overall
platform development process as well. Needless to say that for equal function and performance, the
signal chain in Figure 1(b) has both lower power consumption and smaller form factor than the one
in Figure 1(a).

An instantiation of this technology can be found in Analog Devices’ AD6676 with functional block
diagram shown in Figure 3. The latter is an integrated IF digitization sub-system embedding a
tunable band-pass CT DS with very high instantaneous dynamic range along with digital filtering
and down-conversion functions, automatic gain control support, integrated clock synthesizer and a
JESD204B serial output interface. The center frequency (IF) of the pass-band can be digitally tuned
between 70MHz and 450MHz, and its bandwidth can be programmed to be between 20MHz and
160MHz with varying in-band noise spectral density.

Figure 3: The functional block diagram of Analog Devices’ AD6676.

The performance of this part, as found in its datasheet, makes it suitable for a variety of wideband
cellular infrastructure equipment and repeaters, point-to-point microwave equipment, spectrum
analyzers, communication instrumentation etc.
Conclusions

Important signal chain simplification and performance optimization, increased system design flexibility and reduction in its development effort can be realized when Continuous Time Delta-Sigma ADCs are used. Some of the benefits of these architectures have previously made them commonplace in a variety of low power and mobile applications. Thanks to a number of recent IC technology breakthroughs, CT DS are now also able to meet the stringent ADC high dynamic performance requirements of many communication infrastructure and instrumentation systems while maintaining stable operation in the presence of strong in-band and out-of-band interferers.

An IF sub-system embedding a band-pass CT DS high speed converter with programmable center (IF) frequency and bandwidth combined with a digital down-conversion and filtering post-processing back-end stage, along with other integrated functions, provides a very flexible and powerful solution for software radio applications. Moreover, it also results into overall system level reduction, increased flexibility and performance optimization of the signal chain by further allowing elimination of a number of additional signal conditioning blocks otherwise mandated by mainstream ADC technology.

[1] CT stands for Continuous Time. That’s in contrast with discrete time (DT) circuits, namely sampled data circuits. Delta-sigma (DS) ADCs and modulators can either be CT or DT circuits. In CT DS, the sampling occurs together with quantization after the input signal has been pre-filtered with CT circuitry. Conversely in a DT DS, the input is immediately sampled and then filtered with a discrete analog filter before it is finally quantized.

[2] Or substantially reduces it, depending on the overall system specifications.