Sequential clock gating maximizes power savings at IP level

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1. Introduction

Power Management is one of the major chip design challenges amongst all the dimensions of the design cycle. It poses problems for packaging, portability, & reliability (PPR), e.g., “high system cost of fans – cooling, extending battery life & reduced electron migration” at later stage. Power saving and power dissipation calculation at a higher abstraction level than gate level becomes mandatory in this fast growing and restrictive time to market. Power explorations and its trade-off with area/timing becomes essential at the RTL abstraction level rather than waiting for this data after gate level runs. IP designers have a lot of flexibility to iterate to find ways to meet power budget at this point.

In this paper we talk about design exploration using the PowerPro tool. For analysis of power optimization based on this tool, we have included Advanced Driver Assistance System (ADAS) and cluster IPs with high speed processing requirements. These IPs have multiple complex operation requirements within a clock period, making them ideal candidates for power saving. The IPs under consideration are image processors, high-speed bus fabrics for a memory controller, display controllers, and video codecs.

2. Power of sequential analysis technology in IP Design Flow

Clock gating is the most frequently used techniques as it controls all power consuming components - Reduction in signal/bus toggles, save register and clock tree power. It also covers combinational power if the gate flop is driving large arithmetic operators. Combinational clock gating can’t cover analysis across sequential boundaries. Sequential analysis has the power to analyze the design across multiple cycles to identify redundant writes into a register. Hence, it has emerged as a very powerful technique to identify new clock gating conditions in the design. Manually identifying such opportunities is not easy. Figure-1 demonstrates the power of sequential analysis.
It requires mathematical and formal reasoning to find conditions under which writes to a flop never make their way to the design output or the same data value is getting written over and over to the same flop. In other words, a non-pattern-dependent formal approach is required to discover gating conditions.

### 3. Low Power Methodology Integrated in IP design cycle

Figure-2 shows the typical design flow to adopt the Low Power methodology at IP design cycle.
The PowerPro tool can be used by RTL designers at any time in the design cycle. However the best usage would be to use it in the flow as early as possible to achieve “Design-For-Power” RTL. Cleaning up the clocks for multiple clock domain design is considered as a good practice. Correct selection of Power use case scenario and its filtering is very important. Designers need to make sure that the evaluation of the use case is for maximum toggling for the block. It very well relates the statement - “Power can be saved only where power is consumed”. Designers may also choose to evaluate multiple mode power case based on average design “clock gating efficiency” and effective instances/flop’s efficiency. For complex IPs, designers should use multiple use cases with defined weight to be evaluated for power optimization.

4. Design Exploration for Power

PowerPro clock gating capabilities are used to explore the design for finding clock gating expression. All the suggested expressions by the tool are formally proven. There is also an option to use automated RTL from the tool, but as a RTL designer it is always recommended to know that what is going to be added in the IP rather than using the automated flow. Designer start analyzing the clock gating expression to adopt in RTL. Also, analyze redundant MUX toggles and high toggling signals to fix the wasted power. There are redundant toggle points for instances which helps us in identifying the less efficient part of the design for Power. This helps us in re-architecting the block with proper gating condition. Figure-3 is one example from our IP architecture.

![CRC Block Structure Diagram](image)

Different protocols play around with the CRC calculation on the various phases of data line. Moreover data rate varies on the input data line and the valid data also come in chunks. The line may have valid data for short duration and remain stable for the rest of the time. Clock for the complete CRC calculation module is shut off during invalid data phases. In a nutshell, any free-running clock to the CRC module is avoided.

There are multiple dimensions to adopt the changes in a “Guided” RTL optimization flow:
- Cost-driven Commitment of Sequential Clock Gating
- Weakening gating conditions to reduce area/delay cost

Figure 4: Possible Clock Gating opportunities

Design analysis is done based on the possible clock gating options for sequential path as suggested by PowerPro. The amount of power saving is weighed between the timing criticality and power saved. Figure-4 shows the various possible clock gating options that are reported by PowerPro. Each of the clock gating has clock enable derived from different levels of combinational logic. This allows the designer to have a more flexible clock tree, as the timing criticality of clock enable can constraint the placement of clock-gating cell. Using all these capabilities, a considerable choice of clock-enable and clock-gating cell is chosen.

5. Results and Conclusion

The Low Power flow has been applied across multiple designs IPs. Figure-5 shows the quality-o-results (QoR) across different designs.
Total Design Power Saving varied from 6% to 58% based on IP application and design maturity re power optimization. Clock gating expressions were adopted at different stages of the design cycle based on individual IP design flows. For ADAS and cluster applications in automotive, significant power savings were obtained with no impact to the rest of the design flow, including schedule.

6. References


[2] CDC aware power reduction for Soft IPs, DAC-2014


[4] Clock Gate Logic Aware Design Closure

Also see:
- Recursive clock gating: Performance implications
- Design faults leading to clock and data glitches

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