Silicon debug challenges and guidelines

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Silicon validation is a process of identifying failures resulting from testing during silicon bring-up. During the IC design and manufacturing cycle, manufacturing tests screen out the failed chips. Diagnosis is done to find out why the chips failed, which becomes especially important when the yield is low or when a customer returns a failed chip. With shrinking technology nodes, new types of physical defects arise. This fact makes the diagnostic process quite tricky, difficult, and time-consuming. This article will cover different challenges one faces during silicon debug, and guidelines to be followed to enable faster and more effective diagnosis for ATPG scan test.

Silicon Debug Challenges:

1. **Diagnosis tool limitation**: With the increasing complexity and size of the design, it becomes necessary to increase the compression ratio to reduce test data and test time. Scan compression uses XOR tree to compress the chain data instead of directly observing it. This makes it more difficult for the diagnosis tool to identify the failing flops.

2. **Difficult to figure out diagnosis failures due to incorrect tester setup**: It is possible to have bad calibration on the tester head, resistive connection between the probe-card and chip pads, and a bad package connection.

3. **Difficult to debug failures due to incorrect constraints to generate patterns**: Generally there are a set of design constraints that need to be applied while generating patterns, provided by the design team. If the design team provides different constraints than the ones they used for timing closure, the faulty timing simulation resulted in showing failures on silicon. A closed timing on clock A and selection of clock B would result in timing violation and lead to silicon failure.

4. **Due to test escape chip passes all quality assurance test on silicon but may fail in field testing**: We came across a situation in which all quality assurance tests were passed during silicon bring-up and parts were returned due to failures in field testing. Lack of enough test coverage and advanced fault models will lead to failure in field testing.

5. **Insufficient Margin or passing region on tester**: Every device needs to be tested with 10% Voltage vs. 10% Frequency variation. A good margin would indicate device robustness. Unstable on chip PLL will not generate correct frequency affecting At-speed test and a good margin. Another reason is IR drop due to excessive switching in test mode.

Guidelines for Easy Silicon Debug

1. **Fetch out the list of failing Flops**: The failing flops list needs to be fetched from the tester error log to analyze and locate the faults in the design. Sometimes the ATPG diagnosis tool cannot fetch the failing flop list in compressed mode patterns due to high compression ratio in large SoCs.
Some uncompressed mode patterns need to be applied on the tester to get the failing flops list. The analysis and resolution of the uncompressed mode failure can be applied to compressed mode patterns too.

2. Analyzing and resolving Setup violation: After analyzing the shmoo plot, one can assess the setup violation if applied vectors are passing through lower frequency and higher voltage. Failures would increase if frequency increases as the voltage lowers. This can be considered as setup violation. In the following diagram below of the given shmoo-plot, the green color shows the passing region, other colors depict the number of failures in the shmoo-plot. The setup violation can occur due to real timing violation or due to IR drop. The setup violation can avoided after reducing tester frequency and IR drop can be reduced after using power aware ATPG.

3. Analyzing the Hold violation: One can figure out Hold violation after analyzing the shmoo-plot which is frequency-independent and having failure wall at higher voltage. The occurrence of hold time failures cannot be avoided, once the chip is manufactured. This can be fixed by timing ECO or if failures are on timing exceptions then we can mask them.
4. **Analyzing excessive shift power dissipation:** The device needs to be tested at higher shift frequency to reduce tester time. This causes higher switching activity in shift mode than mission mode, resulting in higher dynamic power dissipation. The following shmoo-plot on the left, gives explanation of chain test failing due to excessive power dissipation. The shmoo-plot on the right shows the chain test after the application of power aware vectors with reduced switching activity.

![Shmoo-plots](image)

5. **First try nominal parts, then slow and fast parts:** Two types of failures occur on the silicon. They are catastrophic failure and parametric failure. The catastrophic failures are functional failures while the parametric failures are caused by the process parameters like voltage, temperature and frequency, which fail to satisfy system requirements. Based on the parameters, the device can be characterized as a fast, slow or nominal device. With silicon testing, the nominal parts need to be tested first. Nominal parts should work on nominal voltage and frequency. The slow and fast parts need to be tested on tester.

6. **At speed test diagnosis:** To debug at-speed test is always challenging, specifically margin issue. The PLL and clock control block make the at-speed test difficult to diagnose. So the stand-alone PLL test vector needs to be verified first to get confidence on the PLL configuration.

7. **Silicon failures due to Model issue:** Sometimes, silicon failures happen due to model mismatch. The model used for ATPG did not match with the real silicon model. One can observe consistent model dependent failures in almost all patterns. Failures would be consistent in number for all voltage vs. frequency variation range across all parts.

**Conclusion**

Silicon failure debug is a critical challenge during project execution. Here, we discussed various silicon debug challenges that one might face, and ways to debug and overcome those challenges. It becomes critical to identify and diagnose tester-level failures within a short time for timely delivery of the product.

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**Also see:**
- [Guidelines improve test quality in advanced CMOS nodes](#)