Editor's note: We continue with Part 2 on this topic. Part 1 can be found [here](#).

**Loop Compensation Design of a Current Mode Converter**

In Figures 16 and 21, the power stage $G_{CV}(s)$ with closed current loop is determined by the selection of power stage components, which are mainly decided by the DC specifications/performances of the power supply. The outer voltage loop gain $T(s) = G_{CV}(s) \cdot A(s) \cdot K_{REF}(s)$ is therefore determined by the voltage feedback stage $K_{REF}(s)$ and compensation stage $A(s)$. The designs of these two stages will largely decide the supply stability and transient response.

![Control Block Diagram for Feedback Loop Design](image-url)
In general, the performance of the closed voltage loop $T(s)$ is evaluated by two important values: the loop bandwidth and the loop stability margin. The loop bandwidth is quantified by the crossover frequency $f_C$, at which the loop gain $T(s)$ equals one (0dB). The loop stability margin is typically quantified by the phase margin or gain margin. The loop phase margin $f_m$ is defined as the difference between the overall $T(s)$ phase delay and $-180^\circ$ at the crossover frequency. A 45-degree or 60-degree minimum phase margin is usually needed to ensure stability. For current mode control, to attenuate switching noise in the current loop, the loop gain margin is defined as the attenuation at $\frac{1}{2} \cdot f_{SW}$. In general, a minimum 8dB attenuation (–8dB loop gain) at $\frac{1}{2} \cdot f_{SW}$ is desired.

**Select Desired Voltage-Loop Crossover Frequency $f_c$**

Higher bandwidth helps obtain fast transient response. However, increasing the bandwidth usually reduces the stability margin and makes the control loop more sensitive to switching noise. An optimum design usually achieves a good trade-off between the bandwidth (transient response) and stability margin. In fact, current mode control also introduces a pair of double-poles $\tau_C$ by the sampling effect of the current signal at $1/2 \cdot f_{SW}$ [3]. These double poles introduce an undesirable phase delay around $\frac{1}{2} \cdot f_{SW}$. In general, to obtain sufficient phase margin and PCB noise attenuation, the crossover frequency is selected to be less than $1/10$–$1/6$ of the phase switching frequency $f_{SW}$.

**Design of the Feedback Divider Network $K_{ref}(s)$ with R1, R2, C1 and C2**

In Figure 16, the DC gain $K_{REF}$ of $K_{ref}(s)$ is the ratio between the internal reference voltage $V_{REF}$ and the desired DC output voltage $V_o$. Resistors R1 and R2 are used to set the desired output DC voltage.

$$R_1 = \frac{K_{REF} \cdot R_2}{1 - K_{REF}} \quad \quad (9)$$

where

$$K_{REF} = \frac{V_{REF}}{V_o} \quad \quad (10)$$

The optional capacitor C2 can be added to improve the dynamic response of the feedback loop. Conceptually, at high frequency, C2 provides a low impedance feed-forward path for the output voltage AC signal and therefore, speeds up transient responses. But C2 may also bring undesirable switching noise into the control loop. Therefore, an optional C1 filter capacitor may be added to
attenuate the switching noise. As shown in Equation 11, the overall resistor divider transfer function
\( K_{\text{REF}}(s) \) with \( C_1 \) and \( C_2 \) has one zero and one pole. Figure 22 shows the bode plot of \( K_{\text{REF}}(s) \). By
designing \( f_{z,\text{ref}} < f_{p,\text{ref}} \), \( C_1 \) and \( C_2 \) together with \( R_1 \) and \( R_2 \) introduce a phase boost in a frequency
band centered at \( f_{\text{CENTER}} \), which is given in Equation 14. If \( f_{\text{CENTER}} \) is placed at the targeted crossover
frequency \( f_{C} \), \( K_{\text{REF}}(s) \) provides phase lead to the voltage loop and increases the phase margin. On the
other hand, Figure 22 also shows that \( C_1 \) and \( C_2 \) increase the divider gain at high frequency. This is
undesirable because a gain increase at high frequency makes the control loop more sensitive to
switching noise. The increase in high-frequency gain by \( C_1 \) and \( C_2 \) is given by Equation 15.

\[
f_{z,\text{ref}} = \frac{1}{2\pi \cdot R_2 \cdot C_2} \quad (12)
\]

and

\[
f_{p,\text{ref}} = \frac{1}{K_{\text{REF}}} \cdot \frac{1}{2\pi \cdot R_2 \cdot (C_1 + C_2)} \quad (13)
\]

\[
f_{\text{CENTER}} = \frac{1}{2\pi \cdot R_2} \cdot \sqrt{\frac{1}{K_{\text{REF}} \cdot (C_1 + C_2)}} = f_{C} \quad (14)
\]

\[
\Delta \text{Gain}_{\text{HF(dB)}} = 20 \cdot \log \left( \frac{G_2}{C_1 + C_2} \cdot \frac{1}{K_{\text{REF}}} \right) \quad (15)
\]
For a given $C_1$ and $C_2$, the increased phase $\phi_{\text{REF}}$ from the divider network can be calculated by Equation 16. Further, the maximum possible phase boost for a given output voltage is given by Equation 17, for $C_2 >> C_1$. As shown, the maximum phase boost $\phi_{\text{REF, max}}$ is determined by the divider ratio $K_{\text{REF}} = V_{\text{REF}}/V_O$. Since $V_{\text{REF}}$ is fixed for a given controller, higher phase boost can be achieved with higher output voltage $V_O$.

\[
\phi_{\text{REF}} = 2 \cdot \tan^{-1} \left( \frac{C_1}{C_1 + C_2} \cdot \frac{1}{K_{\text{REF}}} \right) - 90 \quad (16)
\]

\[
\phi_{\text{REF}} = 2 \cdot \tan^{-1} \left( \frac{1}{K_{\text{REF}}} \right) - 90 \quad (17)
\]

The selections of $f_{\text{REF}}$, $C_1$ and $C_2$ are a trade-off between desired phase boost and undesired high
frequency gain increase. The overall loop gain needs to be checked later for optimized values.

**Design Type II Compensation Network of Voltage-Loop ITH Error Amplifier**

The ITH compensation $A(s)$ is most critical to the loop compensation design because it determines the DC gain, crossover frequency (bandwidth) and the phase/gain margins of the supply voltage loop. For a current source output, $g_m$ transconductance-type amplifier, its transfer function $A(s)$ is given by Equation 18:

$$A(s) = g_m Z_{ith}(s)$$

where, $g_m$ is the gain of the transconductance error amplifier. $Z_{ith}(s)$ is the impedance of the compensation network at the amplifier output ITH pin.

From the control block diagram in Figure 21, the voltage loop regulation error can be quantified by:

Therefore, to minimize the DC regulation error, a large DC gain of $A(s)$ is very desirable. To maximize the DC gain of $A(s)$, a capacitor $C_{th}$ is first placed at the amplifier output ITH pin to form an integrator. In this case, the $A(s)$ transfer gain is:

$$A(s) = g_m C_{th}$$

Figure 23 shows the schematic diagram of $A(s)$ and its Bode plot. As shown, capacitor $C_{th}$ creates an integration term in $A(s)$ with an infinitely high DC gain. Unfortunately, in addition to the original -180 degrees of negative feedback, $C_{th}$ adds another -90 degrees phase lag. Including the -90 degree phase of the 1st-order system power stage $G_{CV}(s)$, the total voltage loop phase is close to -360 degrees at the crossover frequency $f_C$ and the loop is close to being unstable.

In reality, the output impedance of the current source $g_m$ amplifier is not an infinite value. In Figure 24, $R_o$ is the internal output resistance of the $g_m$ amplifier ITH pin. Linear Technology controllers’ $R_o$ is usually high, in the 500kΩ - 1MΩ range. Therefore, the single capacitor $A(s)$ transfer function becomes Equation 21. It has a low frequency pole $f_{po}$ determined by $R_o \cdot C_{th}$. So the DC gain of $A(s)$ is actually $g_m \cdot R_o$. As shown in Figure 24, $A(s)$ still has -90 degree phase lag at the expected crossover frequency $f_{c,exp}$. 
\[ A(s) = \frac{v_{th}(s)}{v_{FB}(s)} = g_m \cdot R_o \cdot \frac{1}{1 + \frac{s}{s_{po}}} \]  

(21)

where,

\[ s_{po} = \frac{1}{R_c \cdot C_{th}} \]  

(22)

**Figure 23:** Step1: Simple Capacitor Compensation Network \( A(s) \) and Its Bode Plot
To increase the phase at $f_c$, a resistor $R_{th}$ is added in series with $C_{th}$ to create a zero, as shown in Equation 23 and Figure 25. The zero contributes up to +90 degree phase lead. As shown in Figure 25, if the zero $s_{thz}$ is placed before the crossover frequency $f_c$, $A(s)$'s phase at $f_c$ can be significantly increased. As a result, it increases the phase margin of the voltage loop.

$$A(s) = \frac{V_{th1}(s)}{V_{FB}(s)} = g_m \cdot R_o \cdot \frac{\frac{1}{s_{thz}}}{1 + \frac{s_{thz}}{s_{po}}}$$  \hspace{1cm} (23) $$

where,

$$s_{thz} = \frac{1}{R_{th} \cdot C_{th}}$$  \hspace{1cm} (24) $$

Unfortunately, there is a penalty of adding the zero $s_{thz}$—the gain of $A(s)$ is significantly increased at high frequency beyond $f_c$. So the switching noise is more likely to come into the control loop with less $A(s)$ attenuation at the switching frequency. To compensate this gain increase and attenuate PCB noise, it is necessary to add another small ceramic capacitor $C_{thp}$ from the ITH pin to IC signal ground, as shown in Figure 26. Typically, choose $C_{thp} << C_{th}$. In the PCB layout, filter capacitor $C_{thp}$
should be placed as close to the ITH pin as possible. By adding $C_{thp}$, the final compensation transfer function $A(s)$ is given in Equations 25 and 26 and its Bode plot is shown in Figure 26. $C_{thp}$ introduces a high-frequency pole $s_{thp}$, which should be located between the crossover frequency $f_c$ and the switching frequency $f_s$. $C_{thp}$ reduces $A(s)$ gain at $f_s$, but may also decrease the phase at $f_c$. The location of $s_{thp}$ is a trade-off between the phase margin and supply PCB noise immunity.

Figure 25: Step 2: Adding $R_{th}$ Zero to Boost Phase — One-Pole, One-Zero Compensation $A(s)$
Figure 26: Step 3: Adding High Frequency Decoupling $C_{thp}$ - Two-Pole, One-Zero Compensation $A(S)$

$$A(S) = \frac{V_{th}(S)}{V_{FB}(S)} = g_m \cdot R_a \cdot \frac{1 + \frac{s}{S_{thz}}}{\left(1 + \frac{s}{S_{po}}\right) \cdot \left(1 + \frac{s}{S_{thp}}\right)} \quad (25)$$

where,

$$S_{thp} = \frac{1}{R_{th} \cdot C_{th} \cdot C_{thp}} = \frac{1}{R_{th} \cdot C_{thp}} \quad \text{if} \quad C_{thp} \ll C_{th} \quad (26)$$

Since the current mode power stage is a quasi-single-pole system, the two-pole and one-zero compensation network in Figure 26 is generally sufficient to provide the needed phase margin.

This two-pole, one-zero compensation network on the amplifier ITH pin is also called a Type II compensation network. In summary, there are two capacitors $C_{th}$ and $C_{thp}$, and one resistor $R_{th}$. This
R/C network together with the amplifier output resistance $R_o$, generates a typical transfer function shown in Figure 27, with one zero at $f_{z1}$ and two poles at $f_{po}$ and $f_{p2}$.

**Figure 27:** Conceptual Plot of Type II Compensation Network Transfer Function

**Compensation R/C Values vs. Load Step Transient Response**

The previous section explained the frequency domain behavior of the Type II compensation network. In a closed-loop supply design, one important performance parameter is the supply’s output voltage undershoot (or overshoot) during a load step-up (or load step-down) transient, which is usually directly impacted by loop compensation design.

1) $C_{TH}$’s effects on a load step transient. The $C_{TH}$ affects the location of low frequency pole $f_{po}$ and zero $f_{z1}$. As shown in Figure 28, a smaller $C_{TH}$ can increase the low-to-mid frequency gain of transfer function $A(s)$. As a result, it can reduce the load transient response settling time without much impact on the $V_{OUT}$ undershoot (or overshoot) amplitude. On the other hand, a smaller $C_{TH}$ means higher $f_{z1}$ frequency. This may reduce the phase boost by $f_{z1}$ at the targeted crossover frequency $f_c$. 
2) $R_{TH}$’s effects on load step transient. Figure 29 shows that the $R_{TH}$ affects the location of zero $f_{z1}$ and pole $f_{p2}$. More importantly, a larger $R_{TH}$ increases the A(s) gain between $f_{z1}$ and $f_{p2}$. As a result, a
larger $R_{th}$ directly increases the supply bandwidth $f_c$ and reduces the $V_{out}$ undershoot/overshoot at load transient. However, if $R_{th}$ is too large, the supply bandwidth $f_c$ can be too high with insufficient phase margin.
3) $C_{THP}$'s effects on load step transient. Figure 30 shows that $C_{THP}$ affects the location of pole $f_{p2}$. $C_{THP}$ is used as a decoupling capacitor to reduce switching noise on the ITH pin to minimize switching jitter. If the supply bandwidth $f_c > f_{p2}$, $C_{THP}$ does not impact load transient response much. If $C_{THP}$ is over-designed so that $f_{p2}$ is close to $f_c$, it can reduce the bandwidth and phase margin, resulting in increased transient undershoot/overshoot.
Design a Current Mode Supply With the LTpowerCAD Design Tool

With the LTpowerCADTM design tool, users can easily design and optimize loop compensation and load transient performance of Linear Technology’s current mode supplies. Many Linear products have been accurately modeled with their loop parameters. First, users need to design the power stage first, in which they need to design the current sensing network and ensure a sufficient AC sensing signal to the IC. After that, on the loop design page as shown in Figure 31, they can adjust the loop compensation R/C values by simply moving the sliding bars and observing the overall loop bandwidth, phase margin and corresponding load transient performance. For a buck converter, users usually need to design a bandwidth below $1/6 \ f_{SW}$, have at least 45 degrees (or 60 degrees) of phase margin and have at least 8dB total loop gain attenuation at $\frac{1}{2} \ f_{SW}$. For a boost converter, because of the right-half-plane zero (RHPZ), users need to design the supply bandwidth below $1/10$ of the worst case RHPZ frequency. The LTpowerCAD design file can be exported to LTspice for real-time simulation to check detailed supply dynamic performance, such as load transient, power-up/down, overcurrent protection, etc.

Figure 31: LTpowerCAD Design Tool Eases Loop Compensation Design and Transient Optimization
The LTpowerCAD and LTspice programs are not intended to replace final bench loop gain measurement of the real power supply. It is always necessary to make a measurement before releasing the design for final production. Though the models of power supplies are theoretically correct, they cannot take full account of circuit parasitics and component nonlinearity, such as the ESR variations of output capacitors, the nonlinearity of inductors and capacitors, etc. Also, circuit PCB noise and limited measurement accuracy may also cause measurement errors. That’s why, sometimes, the theoretical model and measurement can diverge considerably. If this happens, a load transient test can be used to further confirm the loop stability.

Figure 32 shows the typical supply loop gain measurement setup of a nonisolated power supply using a frequency analyzer system. To measure the loop gain, a 50Ω to 100Ω resistor is inserted into the voltage feedback loop and a 50mV isolated AC signal is applied on this resistor. Channel 2 is connected to the output voltage and Channel 1 is connected to the other side of this resistor. The loop gain is calculated as Ch2/Ch1 by the frequency analyzer system. Figure 33 shows the measured and LTpowerCAD calculated loop Bode plot of a typical LTC3851A current mode supply. They have good matching in the critical frequency range from 1kHz to 100kHz.

![Figure 32: Test Setup of the Power Supply Loop Gain Measurement](image-url)
Operating Conditions:

If the supply switching or output voltage waveform looks unstable or jittery on the oscilloscope, first, users need to make sure the supply is operated in a steady state condition, without load or input voltage transients. For very small or very large duty cycle applications, if pulse-skipping operation happens, check whether the minimum on-time or off-time limitation has been reached. For supplies that require an external synchronization signal, make sure the signal is clean and within the linear range given by controller data sheet. Sometimes it is also necessary to adjust the phase-locked-loop (PLL) filter network.

Current Sensing Signal and Noise:

To minimize the sensing resistor power loss, in a current mode supply, the maximum current sensing voltage is typically very low. For example, LTC3851A may have 50mV maximum sensing voltage. It is possible for PCB noise to disturb the current sensing loop and cause an unstable switching behavior. To debug whether the problem is indeed a loop compensation problem, a large 0.1µF capacitor can be placed from ITH pin to IC ground. If the supply is still unstable with this capacitor, the next step is to review the design. In general, the inductor and current sensing network should be designed to have at least 10mV to 15mV peak-to-peak AC inductor current signal on the IC current sensing pin. Besides, the current sensing traces can be rerouted with a pair of twisted jumper wires to check if it solves the problem.

There are some important considerations for PCB layout [6]. In general, Kelvin sensing is usually required with a pair of closely routed current sensing traces back to SENSE+ and SENSE− pins. If a PCB via is used in the SENSE− net, make sure this via does not contact other V_{OUT} planes. The filter capacitor across SENSE+ and SENSE− should be placed as close to the IC pins as possible with a direct trace connection. Sometimes, filter resistors are needed and these resistors must be close to the IC too.

Control Chip Component Placement and Layout:

Placement and layout of components around the control IC are also critical [6]. All the ceramic decoupling capacitors should be close to their pins, if possible. It is especially important for the ITH pin capacitor C_{thp} to be as close to the ITH and IC signal ground pins as possible. The control IC
should have a separate signal ground (SGND) island from the power supply power ground (PGND). The switching nodes, such as SW, BOOST, TG and BG, should be kept away from sensitive small signal nodes, such as current sensing, feedback and ITH compensation traces.

Summary

Loop compensation design is often viewed as a challenging task for switching mode power supplies. For applications with fast transient requirements, it is very important to design the supply with high bandwidth and sufficient stability margin. This is typically a time consuming process. This article explains the key concepts to help system engineers understand this task. The LTpowerCAD design tool can be used to make supply loop design and optimization a much simpler task.

References


[5] LTpowerCAD design tool and user guide.
