Slope Compensation in PCMC DC-DC Converters

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Over the years I’ve run into a number of engineers who haven’t had the chance to fully master the concept of slope compensation in dc-dc converters. I’ll try to clarify [1] this concept using the buck converter as a vehicle. **Figure 1** exemplifies the buck conversion principle. The switch is toggled between the source $V_I$ and ground at a frequency of $f_s$. The corresponding period is $T_s = 1/f_s$, and the portion of $T_s$ during which the switch is in the up position is denoted as $DT_s$, where $D$ is the **duty cycle** ($0 < D < 1$). A PSpice simulation of the circuit with $f_s = 100$ kHz and $D = 0.25$ yields the waveforms of **Figure 2**. Viewing the circuit as a **low-pass filter**, we note that after an initial transient, the circuit achieves a form of **steady state** during which $V_O$ settles around 3 V, though with a small amount of ripple. If we raise $D$ to 0.5, $V_O$ will settle around 6 V, and if we raise $D$ to 0.75, $V_O$ will settle around 9 V.

![Figure 1](image1.png)

**Figure 1** (a) Buck conversion principle ($f_s$ and $D$ represent the frequency and duty cycle with which the switch is being toggled). (b) $V_O$ as a function of $D$.

In fact, it is easily seen that $V_O$ settles around the **average** of the square-wave denoted as $v_{sw}$ in **Figure 1**, which is

$$V_O = DV_I$$  \hspace{1cm} (1)

Since $0 < D < 1$, it is apparent that the circuit acts as a form of **voltage divider**, with **Equation (1)** holding regardless of the current demanded by the load $R_L$. Initially, a good portion of the inductor current goes into charging up $C$, but once the circuit reaches its steady state, the capacitor current will average to zero, so the average current $I_L$ supplied by the inductor will equal the average
current $I_o$ demanded by the load. In the above example, $I_l = I_o = V_o/R_L = 3$ A.

Figure 2 PSpice waveforms for the circuit of Figure 1 for the case $f_s = 100$ kHz and $D = 0.25$.

The most popular application of the buck converter is the regulation of $V_o$. To regulate, the circuit of Figure 1 must include a controller to sense $V_o$ and to continuously adjust $D$ so as to maintain $V_o$ at a prescribed value regardless of possible variations in $V_i$. Needless to say, the controller is a negative-feedback system. The $RLC$ values of Figure 1 were deliberately chosen for a critically damped transient, but the $RLC$ circuit in use will not necessarily be critically damped, so it is the responsibility of the controller to provide sufficient phase margin to ensure adequate regulator dynamics.

How does the controller adjust $D$? There are two classes of controllers, voltage-mode and current-mode controllers. The following discussion will address a popular subclass of the latter, namely, peak-current-mode control, or PCMC, an example of which is depicted in Figure 3. To sense the inductor current $i_L$, the circuit uses a small series resistor $R_{sense}$, whose voltage drop is then magnified by an amplifier having a gain of $a_I$. This amplifier converts $i_L$ to the voltage $R_i i_L$, where

$$R_i = a_I R_{sense}$$

is the overall gain of the current-to-voltage conversion, in V/A, or ohms. To sense the output voltage $V_o$, the circuit uses the voltage divider $R_1-R_2$ to generate the voltage $\beta V_o$, with
Central to the system is the error amplifier $EA$, a high-gain amplifier that compares $\beta V_o$ against a reference voltage $V_{REF}$ and outputs whatever voltage $v_{EA}$ it takes to make their difference approach zero, thus giving

$$V_o = \left(1 + \frac{R_2}{R_1}\right)V_{REF}$$

(4)

Once it reaches its steady state, the circuit operates as follows:

A cycle initiates when a clock pulse sets the flip-flop. This closes the $M_p$ switch to make $v_{sw} = V_i$. During this portion of the cycle, denoted as $DT_s$ in Figure 4, the inductor current $i_L$ ramps up with a slope of $S_n$ governed by the $i_L$-$v_L$ inductor law, or $S_n = di_L/dt = v_L/L$. During this time we have $v_L = V_i - V_o$, so

$$S_n = \frac{V_i - V_o}{L}$$

(5)
Turning back to Figure 3, we observe that the CMP comparator continuously compares the voltage \( R_i L \) against the voltage \( v_{EA} \), and that as soon as \( R_i L \) reaches \( v_{EA} \), the CMP trips to reset the flip-flop. Dividing both sides by \( R_i \) this is equivalent to saying that the CMP trips as soon as \( i_L \) reaches the value

\[
i_{EA} = \frac{v_{EA}}{R_i}
\]  

This allows us to visualize a cycle exclusively in terms of currents as in Figure 4. Now, resetting the flip-flop opens the \( M_p \) switch while closing the \( M_n \) switch to make \( v_{SW} = 0 \). During the remainder of the cycle, denoted as \((1 - D) T_s\), we have \( v_L = 0 - V_o \), so \( i_L \) ramps down with a slope of \( S_f \) such that

\[
S_f = \frac{-V_o}{L}
\]  

A new cycle begins with the arrival of the next clock pulse.

Two Flaws of Uncompensated PCMC

As is, the circuit of Figure 3 suffers from two flaws. The first flaw is depicted in Figure 5 for the case of a converter designed to regulate \( V_o \) at 3.0 V (for simplicity, a cycle is assumed to start at \( t = 0 \)). Figure 4a shows the steady-state inductor current \( i_L \) and its average \( I_L \) for the case \( V_i = 9 \) V, corresponding to a duty cycle of \( D = 3/9 = 1/3 \). Suppose now \( V_i \) drops to 4.5 V, corresponding to a duty cycle of \( D = 3/4.5 = 2/3 \). Assuming \( v_{EA} \) hasn’t had time to change appreciably, the average inductor current \( I_L \) will rise as in Figure 5b. This is so because while the down-slope \( S_f \) remains constant at \(-3/L\), the up-slope \( S_u \) decreases from \((9 - 3)/L\) to \((4.5 - 3)/L\), that is, from \(6/L\) to \(1.5/L\).
With an increased $I_L$, $V_o$ will also tend to increase, indicating poor regulation.

![Figure 5](image)

**Figure 5** The inductor current of the circuit of Figure 3 for two different duty cycles.

The second flaw is a form of instability known as *sub-harmonic oscillation*, which arises for $D > 0.5$. **Figure 6** shows how an inductor current perturbation $i_i(0)$ at the beginning of a cycle evolves into the perturbation $i_i(T_s)$ at the end of the cycle. (A perturbation might be due, for instance, to a misfiring of the comparator in the course of the previous cycle.) Using simple geometry we can write $i_i(0)/t = S_n$ and $i_i(T_s)/t = S_f$. Eliminating $t$ gives

$$\frac{i_i(T_s)}{i_i(0)} = \frac{S_f}{S_n} = \frac{-D}{1-D}$$

indicating that (a) the polarity of $i_i(T_s)$ is opposite to that of $i_i(0)$, and (b) for $D < 0.5$ its magnitude will decrease to die out after a sufficient number of cycles, but for $D > 0.5$ it will tend to increase from one cycle to the next, leading to the aforementioned sub-harmonic instability.
Slope Compensation

Looking back at Figure 5, we observe that if we want Figure 5b to retain the same $I_L$ value as Figure 5a, we need to reduce the $i_{EA}$ value of Figure 5b so as to “push down” the $i_L$ waveform till the respective $I_L$’s align. By how much do we need to reduce $i_{EA}$? To answer, let us draw the desired $i_L$ waveforms for three different values of $D$. As depicted in Figure 7, top, we start out by drawing the down-ramps for $i_L$, all vertically centered about identical $I_L$’s, and all with the same slope of $S_f = -V_o/L$. Next, we complete the $i_L$ waveforms by drawing the up-ramps, as shown in Figure 7, bottom. Finally, we superimpose the three figures as in Figure 8, and observe that the locus of the peaks defines a ramp with a slope of $S_f/2 = -V_o/2L$. 

Figure 6 Illustrating sub-harmonic oscillation for $D > 0.5$. 

![Figure 6 Illustrating sub-harmonic oscillation for D > 0.5.](image)
Figure 7 Constructing the compensated $i_L$ waveforms for $D = 0.25$, 0.5, and 0.75.

Figure 8 The locus of the peaks of Figure 7 is a ramp with a slope of $S_f/2$. 
This shows precisely by how we must reduce $i_{EA}$, hence the designation slope compensation.

**Figure 9** shows one way of modifying the circuit of **Figure 3** so as to achieve slope compensation. The circuit now includes a saw-tooth generator operating at a frequency of $f_s$, whose output $v_{RAMP}$ is then subtracted from $v_{EA}$ to produce the desired locus of peak values for $i_L$. With slope compensation, the waveforms of **Figure 5** change as depicted in **Figure 10**, where $i_{EA(\text{comp})} = (v_{EA} - v_{RAMP})/R_i$. 

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**Figure 9** Incorporating slope compensation in the PCMC buck converter of Figure 3.
As an added bonus, slope compensation also eliminates sub-harmonic oscillation, as depicted in Figure 11. Using graphical inspection, we observe that a beginning-of-cycle disturbance $i_l(0)$ will result in an end-of-cycle disturbance $i_l(T_s)$ of lesser magnitude, even though $D > 0.5$ (in fact, you can convince yourself that this holds for any value of $D$, $0 < D < 1$). It is the case to say that with slope compensation we are in effect killing two birds with one slope – ops stone. The error amplifier $EA$, shown in Figure 9 as a mere triangle, serves two important functions: (a) to drive its inverting input voltage as close as necessary to the non-inverting one so as to approximate Eq. (4), and (b) to provide a frequency profile suitable to ensure a prescribed phase margin for the whole system. Not at all an ordinary amplifier, which can easily form the body of a future blog on stability analysis and error-amplifier design.
Figure 11 Slope compensation prevents sub-harmonic oscillation regardless of $D$.

References

[1] Design with Operational Amplifiers and Analog Integrated Circuits, Sergio Franco