Chasing 5G: Pizzacato, sigma delta and other architectures

Steve Taranovich - April 16, 2015

In my previous article on EDN, The fully Digital radio transmitter: Is it real or more hype?, there was a great deal of commentary about other alternatives with a digital approach to radio. I these times where we are seriously beginning discussions regarding 5G, I really think that “Outside-th-box” ideas about radically different architectures will emerge to meet the very difficult demands of higher speed and bandwidth radio at much lower power that 5G will need to be successful. So let’s probe a little further into this architecture and see what it might be able to accomplish.

Some of the comments on the previous article mentioned that an all-digital RF transmitter being patented back in the 80s as part of an upstream cable modem design. It used logic gates as the oscillator, amplifier and AM modulator.

Ken Wyatt commented on conversing via CW on the amateur radio band over hundreds of miles by keying the power pin on a digital crystal oscillator fed through a bandpass filter to limit harmonics.

There was also an idea using Raspberry Pi spread-spectrum clock generators available in their standard GPIO block as an FM transmitter.

All of these are alternative radio architectural ideas outside the norm and that’s what I believe it will take for 5G to happen. So ideas like those of Cambridge Consultants for an all-digital radio transmitter will have to be explored and expanded upon as will the one bit ADC and DAC architectures of the Sigma-Delta variety being considered for 5G radios to save power and space at blazing speeds.

First let’s take a further look at Cambridge Consultants Pizzicato architecture. An interesting note is that they started this design with an old, 3Gbps bitstream from a Xilinx Virtex-5 FPGA serdes port. They use a bandpass sigma-delta converter in the bitstream like the early one bit audio sigma-delta devices (We will discuss these later).
A typical modern day radio transmitter architecture starts with a digital data stream into a baseband modulator and on into a high speed DAC, then through filters and an IF mixer that raises the signal to an IF frequency, and through another RF mixer up to the carrier frequency and then amplified by a power amplifier (PA) (Image courtesy of Cambridge Consultants).

Cambridge uses a bandpass sigma-delta converter in the bitstream like the early one bit audio sigma-delta devices (Image courtesy of Cambridge Consultants).

Pizzicato has a few options (Image courtesy of Cambridge Consultants)
High speed 1-bit Sigma Delta Modulators

The NXP white paper in reference 1 states:

*The early audio ADCs sampled at 48 kHz, used single-bit discrete time switched capacitor noise-shaping modulators. Typically the modulators used fourth order loop filters which provided 27 dB/octave low-pass attenuation to push the quantization noise well outside the audio pass band. There it was subsequently filtered by the downstream decimation/low-pass digital filter. These ADCs employed oversampling ratios of 64, and decimation filters that provided more than 90 dB of THD+N, and 95 dB or more dynamic range when producing 16-bit output samples.*

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A block diagram of a first-order analog sigma-delta discrete time modulator, such as would be seen in an audio-band ADC, circa 1995. Note that because the integrators are implemented using switched-capacitor circuits, these sigma-delta converters are considered “discrete time” implementations. (Image courtesy of NXP in Reference 1)

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Tapani Ritoniemi, Tampere University of Technology in Finland, wrote an entire book on this topic entitled *High speed 1-bit Sigma Delta Modulators*. He states that using a high speed 1-bit quantizer sigma delta modulator topology, a 14-bit dynamic range can be achieved with an oversampling ratio of 16 by using cascaded high-order 1-bit delta sigma modulators. The noise transfer function of this block can be modified by placing zeroes in the baseband.

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I remember when a 12 bit, 10 MHz ADC had to be in a large hybrid can with separate sample and hold on a ceramic substrate with a whole slew of discrete components with wire-bonds back in 1988. Then we moved to pipelined ADCs that finally were able to be designed into a monolithic circuit; SARs could not get the high sample rates and bandwidths until fairly recently. Now, the high speed
delta sigma architecture is being given a serious look.

NXP states\(^1\) that in today's modern multi-standard, multi-carrier, multi-band base station infrastructure signal bandwidths are in the 100MHz to 125MHz region. Using a dual-channel ADC at 14 or 16 bits would be in a synchronized I/Q sampling architecture. If high IF frequencies are to be digitized after some antenna signal down conversions, the ADC to digitize these signals would need more than 85 bBc of SFDR and greater than 77 dBFS of SNR. Right now the data interface of choice is JESD204B for lowest power data transmission to the digital realm as well as smallest board footprint for data lines at a rate of 10 to 12 Gbps. 5G would demand far greater sampling rates and bandwidths.

Further ideas

Further ideas abound in the study of Software Defined Radio (SDR) architectures. Reference 2 looks at the ADC problem a little differently. They claim that the critical requirement for Delta Sigma Modulators (DSMs) is high-frequency processing and not a high-oversampling ratio.

In Reference 3, the authors show that the bandwidth of the delta sigma modulator (DSM)-transmitter can be improved using low complexity time-interleaved DSM. The high clock speed requirement of DSM is the main limitation to increase the signal bandwidth in DSM-transmitter. In their research, the bandwidth of DSM-transmitter was increased 4 times by using low complexity four-branch time-interleaved parallel DSM without the need of increasing clock speed. Their low complexity parallel DSM is designed based on a polyphase implementation technique. Then, the transmitter architecture is simulated using MATLAB Simulink and Advanced Design System (ADS).

For this simulation, the uplink long-term evolution (LTE) signal with different bandwidths up to 7.68 MHz is used. The simulation shows that by using four-branch time-interleaved parallel DSM in transmitter architecture for 7.68 MHz LTE signal with oversampling ratio (OSR) of 16, the signal to noise and distortion ratio (SNDR) is about 41 dB with the clock speed of only 30.72 MHz. This is 4 times lower than the required clock speed of the conventional transmitter to achieve the same SNDR.

In reference 4 the authors develop a wideband delta sigma modulator for GHz transceivers for SDR. Their architecture is a delta sigma modulator, a high speed multiplexer and a switching-mode power amplifier (PA). They use a parallel processing time-interleaved architecture to increase the bandwidth of the digital transmitter by a factor of eight and are able to still maintain signal quality. The SNDR was 60 dB.

Far more sampling speed, bandwidth and dynamic range enhancements obviously need to be done in order to approach 5G demands. We need to pursue other such ideas that think “outside-the-box” like these.
Stay tuned to EDN for my coming 5G feature article that will discuss challenges that semiconductor suppliers need to overcome to reach the heights of 5G reality.

**References**

1. [Next generation high-speed sigma-delta ADC architectures](#), NXP white paper

2. Single-Bit Pseudoparallel Processing Low-Oversampling Delta-Sigma Modulator Suitable for SDR Wireless Transmitters, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 22, NO. 4, APRIL 2014

3. Bandwidth Enhancement in Delta Sigma Modulator Transmitter using Low Complexity Time-interleaved Parallel Delta Sigma Modulator, Nasser Erfani Majd, Hassan Ghafoorifard, Abbas Mohammadi

4. TIME-INTERLEAVED DELTA-SIGMA MODULATOR FOR WIDEBAND DIGITAL GHz TRANSMITTERS DESIGN AND SDR APPLICATIONS, M. M. Ebrahimi, M. Helaoui, and F. M. Ghannouchi