The power electronics industry and the semiconductor industry, inseparably intertwined with one another, are facing unprecedented efficiency, cost, construction and thermal challenges which provide many opportunities for innovation. These industries are in the focal point of the “energy challenge” a multifaceted problem that involves mobile and cloud infrastructure systems, Internet-of-Things, renewable energy, smart grid, vehicle electrification, and across-the-board power efficiency enhancements in order to keep up with the IT industry’s rapid growth in data consumption. These are the competitiveness and sustainability challenges of the twenty-first century.

The paradigm shift we have been experiencing in semiconductor packaging technology was brought about by advanced deep submicron semiconductor technology reaching a “cost barrier” that prevented further cost reduction by reducing transistor size and adding more functions to the semiconductor die. This barrier was circumvented through the development of wafer thinning that enabled through-silicon-via (TSV) technology, and the eventual introduction of 2.5D and 3D integration that facilitated heterogeneous (“More than Moore”) integration. It will allow the power requirements of the digital load to increase 2 to 5 times, within the same footprint, in a single generation. The power sources community must now find ways to package power sources that will meet this demand, but with no increase in footprint.

In parallel power semiconductor technology is facing a “construction barrier” that prevents realization of the huge benefits new technology can offer in terms of increased power efficiency and higher power density. These new technologies include gallium-nitride (GaN), silicon-carbide (SiC), and gallium-arsenic (GaAs) power semiconductor devices that require operation in an environment that is free of bond wires and minimizes parasitic interconnect elements. The leading packaging technology to achieve a significant reduction in parasitics (L, R, and C) is embedding active and passive components in printed circuit boards (PCBs) and using packaging technologies developed for 2.5D and 3D integration by the semiconductor industry, outsourced semiconductor assembly and test (OSAT) services, and original equipment manufacturers (OEMs). Thus existing 2.5D and 3D integration and component embedding becomes a key enabling technology for high density power sources utilizing these new power semiconductor devices.

These multiple factors, led the Power Sources Manufacturing Association (PSMA) Packaging Committee to commission a power packaging study that would focus on 3D Embedded Technology.
for Power Packaging. PSMA commissioned LTEC Corporation to execute the study from May 2014-February 2015. The 336 page report “Current Developments in 3D Packaging with Focus on Embedded Substrate Technologies” was derived from the research of over 740 published articles, interviews with 30 industry and academic experts, and attendance at 10 trade shows. The purpose was to determine the availability of imbedded substrate technology usable today and in the future by the Power Industry.

The report is intended to assist executives and engineers in their own analysis of how currently available materials and processes could be best used for the creation of advanced high efficiency, high power-density power sources. The report builds upon the findings of the Phase I report (“3D Power Packaging”) executed by Tyndall National Institute and issued by the Power Sources Manufacturers Association (PSMA) Packaging Committee in 2014. This article will present the strategic observations and implications based on the findings of both reports.

For the purpose of this article the following definitions apply: Embedded substrate technology is defined as the inclusion of at least one active or passive electrical component within the top and bottom conductive layers of a substrate, with a substrate defined as a planar structure having multiple conductive and insulating layers. A 3D Embedded Power Modules is defined as systems that use a combination of at least one controller/driver IC, at least one active component in the power train, and associated interconnect means, embedded in a single package, where the Z-axis is used to reduce footprint and increase power density. Embedded substrate technology example

Figure 1 provides an example of this technology based on Shinko Electric Industries Co.’s (Shinko) Molded Core embedded Package (MCEP®) process:

![Figure 1: Example of embedded substrate technology (Shinko MCEP®)](image)

As part of the project 30 companies were surveyed to determine why they were actively producing or developing power sources utilizing embedded technology and at what power level they were considering for this technology. Figure 2a shows the overriding reasons for using the technology was to reduce size (increase power density) and improve performance. Figure 2b illustrates activity at power levels up to and exceeding 1000 Watts.

![Figure 2a: Motivations for embedded substrates](image)
The core technology required for embedding is a PCB or Inorganic Substrate. Europe is leading in high volume, commercially viable embedded manufacturing technology for power sources. This success was enabled by research projects funded by the European Union's sixth and seventh framework programs (FP6, FP7). The first, "HIDING DIES" (FP6), developed the fundamental technology for chip-in-polymer packaging based on embedding thinned silicon in resin coated copper (RCC) dielectric followed by laser drilling of via holes to the chip contacts and to the substrate and finally metallization of vias and conductor lines. A follow-on project "HERMES", under FP7, focused on bringing the technologies into real manufacturing PCB production. AT&S leveraged its involvement with these programs to develop their large panel-based PCB process known as Embedded Component Packaging (ECP™). The AT&S ECP™ process is depicted in Figure 3. AT&S manufactures on 18 in. x 24 in. panels, has shipped over 100-million units, and claims > 99% yield. Their process is used by Texas Instruments and GaN Systems for embedding of their semi-conductor devices and is planned for the introduction of half-bridge and full-bridge products.

**Figure 3: AT&S Embedded Component Packaging (ECP™) Process Flow**

**TDK-EPC process**

TDK-EPC Corporation has developed its own process named Semiconductor Embedded in Substrate (SESUB™). Their embedded process is suitable for high density power supply modules or subsystems, either as substrates or interposers, with or without over-molding. A benefit of SESUB™ is the ability to have complete metal shielding of the package, an attractive feature for EMI reduction. Figure 4 shows cross-sections of TDK’s SESUB™ process.

**Figure 4a: Shows the cross-section of TDK’s embedding process with components mounted on top.**

**Figure 4b: The cross-section of an over-molded, shielded power management unit (PMU).**

General Electric has been a pioneer in recognizing the benefits of component embedding and in technology development, beginning with technology for chip embedding in the 1990’s. GE’s “chip-first” technology evolved over several years as a polyimide-based Cu-plated embedding platform compatible with products ranging from high density I/O to power products and RF devices and...
subsystems. This technology has evolved into a process known as GE’s Power Overlay Technology (POL), backed by a strong portfolio of over 300 patents. The POL process begins with 0.5 mil to 5.0 mil polyimide film laminated to a metal frame. The film is coated with adhesive formulated to be compatible a lased drilling process. Next, the semiconductor dies with solderable metallization are placed face down, the adhesive is UV cured, and polyimide layer and the cured adhesive are laser drilled to create micro-via openings from the side opposite to the die. Next, adhesion layer and Cu seed layer are deposited, followed by Cu plating, via filling, patterning, and etching. Build-up layers are added as dictated by interconnect requirements. Subsequent process steps depend on the particular package variant (ePOL, WPOL, POL-MCM, POL-kW, etc.) chosen. Additional standard process steps, such as over molding, solder ball placement or Cu pillar/pad formation, may be added to the manufacturing flow. GE’s POL planned family and process is summarized in Figure 5.

**Figure 5: General Electric Corporation’s POL family, and simplified process summary**

GE’s POL platform also offers advantages of reduced parasitic interconnect inductances and good thermal properties through the replacement of bond wires with direct Cu-plated connection to the die. The semiconductor die can be sandwiched between Cu layers on both sides of the die, allowing a double sided thermal path. Internal EMI shielding is also practical. However, since plasma and sputtering processes are required, the POL technology is not transferable directly to standard PCB fabrication facilities. GE’s selection of polyimide-based technology reflects their emphasis on meeting requirements of high reliability military, aerospace, medical, and industrial applications. GE is actively engaged in licensing its technology as a means of developing the supply chain and enhancing the probability of successful volume manufacturing.

**Infineon variant**

Infineon was a participant in the EU funded FP6, FP7 programs, supporting AT&S in the development of their process. However, they subsequently developed a variant that is similar to TDK-EPC’s SESUB™ and have used that in their Dr. Blade™ process and product family, for which a simplified process illustration is provided in Figure 6.

**Figure 6: A simplified view of Infineon’s Dr. Blade™ process**

Schweizer AG’s P²-PAK process was an early entrant to embedding developed as an alternative to expensive direct-bond-copper (DBC) for inverters, converters, industrial motor drives, and automotive applications. Their process begins with a Cu lead frame sheet with openings for semiconductor die that is placed on an insulating layer. A layer is added above the lead frame once semiconductors are placed using conventional PCB fabrication techniques, followed by lithography and etching for top-side die interconnect. Schweizer has also developed lower power embedding
technologies.

Shinko’s MCEP® process was shown in Figure 1. This was not intended to depict a complete list, additional processes from Fujikara, Wurth Electronik, and Semikron are covered in the technology report.

The second key technology for embedding is the availability of components. There are two classes of embedded components. First, there is the discrete device, termed the “inserted” component. In this case, the surface mount passive device, R L or C, is manufactured prior to assembly in the printed circuit board. Usually these are mounted in laser machined cavities within the printed circuit board. Semiconductor devices are also inserted and connected to the substrate using a variety techniques.

Secondly there is the “formed” component that is manufactured as element(s) within the printed circuit board. All three types of passives (Resistors, Capacitors and Inductors) can be formed in an imbedded substrate. Figure 7 illustrates the various types of embedded components. Figure 8 shows how they can be implemented as a PCB substrate.

The ability to execute an embedded power design is very dependent on the availability of inserted passive components, optimized for PCB embedding purposes. The report devotes individual chapters to resistors, capacitors and inductors. Availability of power devices is still somewhat limited in terms of form factor and terminal metallurgy but the number of sources is expanding rapidly. The report also provides lists of vendors with production parts available now.

Successful transition to full volume manufacturing depends on advances in supply chain and technology for compatible passive component technologies. While this article focused on embedded substrate component technology, the 3D Embedded Substrate Technology report also covers the current state of the art as well as challenges and constraints in semiconductors, passive components, high temperature die-attach, interposers, thermal management, packaging technologies, additive manufacturing and laser fabrication, all of which will play a role in the success and timing of a transition to 3D power packaging.

Another sign of the maturing of embedded substrate technology is the number of standards completed and being written. As you can see from the list below many standards now exist. Substrates, components and manufacturing processes are in existence or being developed to meet these standards. There is more elaboration on standards in the report.

- **IPC-2316**: Design Guide for Embedded Passive Device Printed Boards
- **IPC-4811**: Specification for Embedded Passive Device Resistor Materials for Rigid and Multilayer Printed Boards
In summary, there has been substantial progress and excellent opportunities lie ahead for the power electronics and semiconductor industries and the entire manufacturing ecosystem to embrace PCB embedding and 3D packaging technologies for power electronic applications. The intersection of these technologies with the emerging wide-bandgap power semiconductor technology creates truly exciting possibilities at the same time the power electronics industry faces unprecedented challenges to help mitigate the fast growing demand for power. 3D embedded substrate power packaging technologies are, and will be deployed in everything from cell phones to Hybrid Electric Vehicles. These technologies, combined with wide-bandgap semiconductor devices will literally revitalize the entire power electronic infrastructure block by block, module by module, for the twenty-first century.

The PSMA reports on 3D packaging are provided free of charge to PSMA members. Others interested in the reports may order a copy from PSMA at [http://www.psma.com/publications](http://www.psma.com/publications).