A SPLL (software phase-locked loop) is used in this Design Idea to generate a synchronous reference to common-mode powerline interference in two-electrode ECG amplification. Though intended for ECG signal processing, it can easily be adapted to various DSP applications where frequency synchronization is a must.

The basic SPLL structure consists of three blocks: Phase detector (PHD), Loop filter (LF), and Digitally-controlled oscillator (DCO) (Figure 1). The input signal $V_{in}$ is processed in digital form: the PHD is a multiplier – its output, the product of two signals: the input sine wave ($f_{in}$), and the DCO sine output ($f_{ref}$). Sine wave mixing is preferable when low jitter is a must.

The LF integrates the PHD output data in time and increases the resolution due to averaging, so the $m$-bit wide DCO input can be larger than the $n$-bit wide signals.

The DCO operates as a digital-to-frequency converter with sine output, and must be able to match the expected input frequency range.

Figure 1  Software PLL structure
The key part of the SPLL is the loop filter. It must be carefully designed to provide stable system response with appropriate settling time.

Loop gain analysis and design methodology of the SPLL is given in [1], where it is shown how the SPLL z-domain transfer function can be derived from its analog s-domain prototype using backward difference s-plane to z-plane mapping.

The SPLL control loop consists of two integrators: one is hidden in the DCO, and another one is in the LF. Because the LF integrator serves a second integrator in the loop, it must be bypassed with a forward path to maintain stability, as seen in Figure 2. The disadvantage of this topology is that the forward path increases the remaining ripple at the DCO input, which is converted to jitter at the DCO output. The problem can be overcome with a comb filter with notches at all powerline harmonics. The simplest comb filter rejecting all harmonics is a one-period moving-average filter (averager) [2]. Adding this to the loop greatly reduces the remaining ripple at the DCO input, and this is the heart of the Design Idea.

The LF transfer function is given with Eq. (1), where the first multiplicand is the transfer function of the averager, and the second multiplicand is the transfer function of the bypassed integrator:

\[
LF(z) = \frac{T(1 - z^{-1})}{T_{PL}(1 - z^{-1})} \cdot \frac{k_i + k_z (1 - z^{-1})}{1 - z^{-1}}
\]  

\(T\) is the sampling period: \(T = 1/f_s\), \(T_{PL}\) is the powerline period: \(T_{PL} = 1/f_{PL}\). \(k_i\) and \(k_z\) are the gain coefficients in the integrator and in the forward paths. For sampling rate \(f_s = 2\,\text{kHz}\) or \(T = 0.5\,\text{ms}\), \(f_{PL} = 50\,\text{Hz}\) (\(T_{PL} = 20\,\text{ms}\)), \(k_i = 1/128 \times 0.0078\), and \(k_z = 8\), Eq. (1) can be rewritten as Eq. (2):
The LF transfer function, given with Eq. (1), can be realized with the signal flow schematic shown in Figure 2.

The SPLL is implemented and tested on the STM32F407 microcontroller, running at \( f_{\text{clk}} = 100 \text{MHz} \). The microcontroller incorporates a 12-bit ADC which is used to convert the input signal at sampling rate \( f_s = 2 \text{kHz} \). One LSb corresponds to \( 3V/4096 = 0.732 \text{mV} \). The DCO range is \( \pm 2 \text{Hz} \). It is controlled with a 12-bit word; thus, the DCO sensitivity is \( 1 \text{mHz/LSb}, \text{ or } 1.36 \text{Hz/V} \). To avoid floating point multiplications, the DCO generates a 256-level sine wave. The mixer output is divided by 256 to set the correct loop gain. To minimize the DCO's remaining ripple, the ADC sampling rate is a multiple of the generated frequency \( f_{\text{ref}} \). Thus, the averager, included in the LF, is maximally effective in rejection the powerline harmonics.

Figure 3 shows actual operation of the microcontroller. The data are transferred to a PC and visualized with MATLAB. The loop speed depends on the input signal amplitude. It can be seen that the DCO has a stable response with input amplitudes from \( 0.2 \text{V}_{\text{p-p}} \) to \( 1.6 \text{V}_{\text{p-p}} \). Once the DCO input has settled, the generated rectangular waveform leads the input sine wave by 90 degrees.

\[
LF(z) = 0.025 \frac{1-z^{-40}}{1-z^{-1}} \cdot \frac{0.0078 + 8(1-z^{-1})}{1-z^{-1}}
\]  

(2)

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b) $V_{in} = 0.6V_{pp}$, $f_{in} = 50\text{Hz}$

c) $V_{in} = 1.6V_{pp}$, $f_{in} = 50\text{Hz}$
Figure 3: Practical results. For each image, the top display shows input & output signals. The

d) $V_{in} = 0.6V_{pp}, f_{in} = 49\text{Hz}$

e) $V_{in} = 0.6V_{pp}, f_{in} = 51\text{Hz}$
second and third displays are the DCO input at different zooms.

- Download the source code

References:

2. Dobrev D., Simulate digital filters with PSpice, EDN, 2015

Also see:

- Two gates and a microprocessor form digital PLL
- Sine reference is synchronous with ac line
- Adaptive Schmitt trigger tames unruly signals