All you need to know about MIPI D’PHY RX

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MIPI D’Phy, a physical serial communicating layer connecting the application processor to the display device or the camera, offers advantages as the physical layer.

The MIPI (Mobile Industry Processor Interface) alliance is a non-profit organization that establishes standards for hardware and software interfaces in mobile devices. Its vision is to develop the world’s most comprehensive standard set of interface specifications for mobile and mobile influenced products which will maximize design reuse, drive innovation, reduce time to market and will help in interoperability of products from various companies.

MIPI D’Phy is a physical serial data communication layer on which the protocols like CSI (Camera Serial Interface), DSI (Display Serial Interface) runs. It physically connects the camera sensor to the application processor (for CSI) and application processor to the display device (for DSI) as shown in the figure above.

D’Phy is a high speed, low power, source synchronous physical layer which is best suited for power hungry battery operated devices due to its power efficient design. It includes in it both the high speed and low power modules which helps in achieving power efficiency. The payload data (image data) uses the high speed modules whereas the control and status information is send (between
camera/display device and the application processor) with the help of low power modules (utilizing low frequency signals). It has a peculiar ability of sending the high speed and low power data in the single packet burst. The low power modules help in achieving power savings and the high speed modules help in achieving the much needed higher bandwidth requirement for the High definition picture quality data signals.

**Architecture of D'Phy**

In order to meet the high bandwidth requirement of HD quality images, MIPI D’Phy consists of one clock lane and has an option of configurable number of data lanes with a maximum of four lanes. The bandwidth can be increased by increasing the number of data lanes. By increasing the number of lanes, the same quantity of data can be transmitted on multiple lanes in lesser time. MIPI D’Phy uses forward source synchronous clock, which is used by all the data lanes of D’Phy receiver for capturing the high speed data signals.

In order to meet both the low power and high speed requirements, every data lane of universal D’Phy IP (as shown in the above figure) consists of low power transmitter (LP-TX), high speed transmitter (HS-TX), serializer for transmitting MIPI D’Phy specific patterns and on receiving side it consists of low power receiver (LP RX), high speed receiver (HS-RX), deserializer and a low power contention detector (LP-CD) for receiving those MIPI D’Phy specific data signals.

The clock lane consists of the low power transmitter (LP-TX), high speed transmitter (HS-TX) for transmitting MIPI D’Phy specific clock lane patterns and on receiver side it consists of low power
receiver (LP RX), high speed receiver (HS-RX) and a low power contention detector (LP-CD) for receiving those MIPI D'Phy specific clock signals.

Every data lane (or clock lane) of the receiver is connected to the transmitter through two wires, Dp and Dn (or Clkp and Clkn). Both high speed and low power data transmission happens on these two wires connecting these two communicating modules.

The Low power module, an unterminated module, operate in single ended manner and work on 1.2V logic voltage. The data rate of low power signals, used for providing control and status information, is less than 10Mbps.

The high speed modules operate in a differential manner. They utilize the low voltage swing of the payload data signals to transfer the information (typical differential output swing -- Dp – Dn -- of high speed signals is 200mV). It contains usually an on die termination, of value, typically 100 ohm differential (between Dp and Dn).

**Working of D’Phy and data flow between camera output to MIPI D’PHY receiver**

The image data captured by the camera sensor is processed by the MIPI transmitter to be transmitted over its multiple data lanes. The number of data lanes to be used for the transmission of data is configurable.

Depending on the number of data lanes to be used for data transmission, the image data is organized by the transmitter. The transmitter then serializes the data on each lane and transmits it to the corresponding receiving lanes.

For example, if two lanes are used, the first byte of payload data is sent over data lane 0 and second byte on data lane 1. Similarly, on the receiving side, the serial data from each data lane is converted into byte format with the help of deserializer present in each receiving lane of the D’Phy. After this, the deserialized bytes from each lane are merged together by the CSI controller.

Before the payload data of every HS burst on each lane, the transmitting D’Phy inserts a sync sequence (00011101) as shown in the below figure. This sync sequence is used by the data lanes of the receiving D’Phy to establish synchronization with the high speed payload data. It is only when the synchronization signal is properly decoded by the receiving D’Phy, the payload data is forwarded to the MIPI CSI 2 controller for further processing of the data.
As part of the initialization of D’Phy, initially all the lanes are held at LP11 state (1.2V level) for a specified time. This LP11 state is also known as stop state. After this, for sending the image data, the transmitter drives a particular sequence on the receiver to enter the receiver lanes from the low power mode to high speed mode. The high speed entry sequence consists of driving LP11->LP0->LP00 (LP->HS transition) on the receiver lanes as shown in the following figure. On successful reception of this sequence the high speed receiver module enables its termination to receive the high speed differential data.

Now the high speed receiver termination has become active and the receiver starts to receive the high speed data from the transmitter. However, after LP->HS transition, the transmitter sends HS Zeros (V(Dn)>V(Dp)) for a specified amount of time to make sure that the receiver is enabled properly before any payload data is transmitted.

Once enabled, HS receiver continues to receive the data till it encounters the LP11 state on its lane. The LP11 state brings back the data lane from high speed mode to low power mode.
The payload data transmitted over the D’Phy data lane is in packet format. It could be either a long packet or a short packet. Long packet consists of 32 bit Packet header, payload data and 16 bit of packet footer. Short packet consists of 32 bit of packet header only.

After every HS burst the data lanes go to LP11 state. A single HS burst represents the image data corresponding to one of the horizontal line of an image and the LP11 state in-between the HS bursts represents the blanking periods. Because low power commands require signals to be send at lower frequency, this intermittent movements of D’Phy in LP and HS modes helps in reducing the overall power consumption.

When no data transfer is required, all the lanes are kept in ULPS mode (ultra-low-power mode). This is a special low power mode which helps in further reducing the power. ULPS mode is entered through a specific low power pattern. Once in the ULPS state all the lanes are driven low (0V). The ULPS entry pattern are different for clock and data lanes.

**Timing relationship between differential clock and data**

The high speed payload data from the transmitter is transmitted on both the edges of the High speed differential clock (DDR clock) as shown in the below figure. The high speed differential clock and the data transmitted from the transmitter are 90 degrees out of phase and with the data being transmitted first. This timing relationship between clock and data helps in achieving the setup and hold time requirements at the receiver data lanes.
Conclusion

MIPI D'Phy as a physical serial communicating layer is gaining traction in the today’s power hungry mobile and mobile related applications due to its low power consumption operation.

Also see:

- Manage EMI from high-speed digital interfaces
- How to test for MIPI M-PHY compliance