FPGA IP cores enable flexible SoC design

Susan Nordyk - September 13, 2015

Optimized for TSMC’s 28-nm process, Menta’s predefined off-the-shelf IP cores for complex SoC devices simplify post-production customization. The eFPGA (embedded FPGA) IP cores, together with the Menta Origami programming tool suite, allow designers to make post-fabrication changes quickly and easily.

The family of IP cores includes six new eFPGA options that provide from 4,000 to 60,000 equivalent ASIC gates, plus DSP blocks. IP cores are delivered as hard macros with optimized array sizes for embedded logic blocks, embedded custom blocks, and embedded memory blocks, each of which are customizable in type, number, and size to address various markets and applications.

eFPGA IP cores are designed for standard test compatibility with all common ASIC and SoC test solutions, featuring fault coverage of up to 99.8%. The cores are enabled and configured using Origami EDA tools. Origami encapsulates all the necessary design steps of classical FPGA design flow, from netlist to the programming bitstream with synthesis, mapping, place, and route. Synthesis allows RTL applications in VHDL, Verilog, or SystemVerilog.
Menta, www.menta-efpga.com

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